

Compal Confidential

FLMS0

DIS M/B Schematic Document

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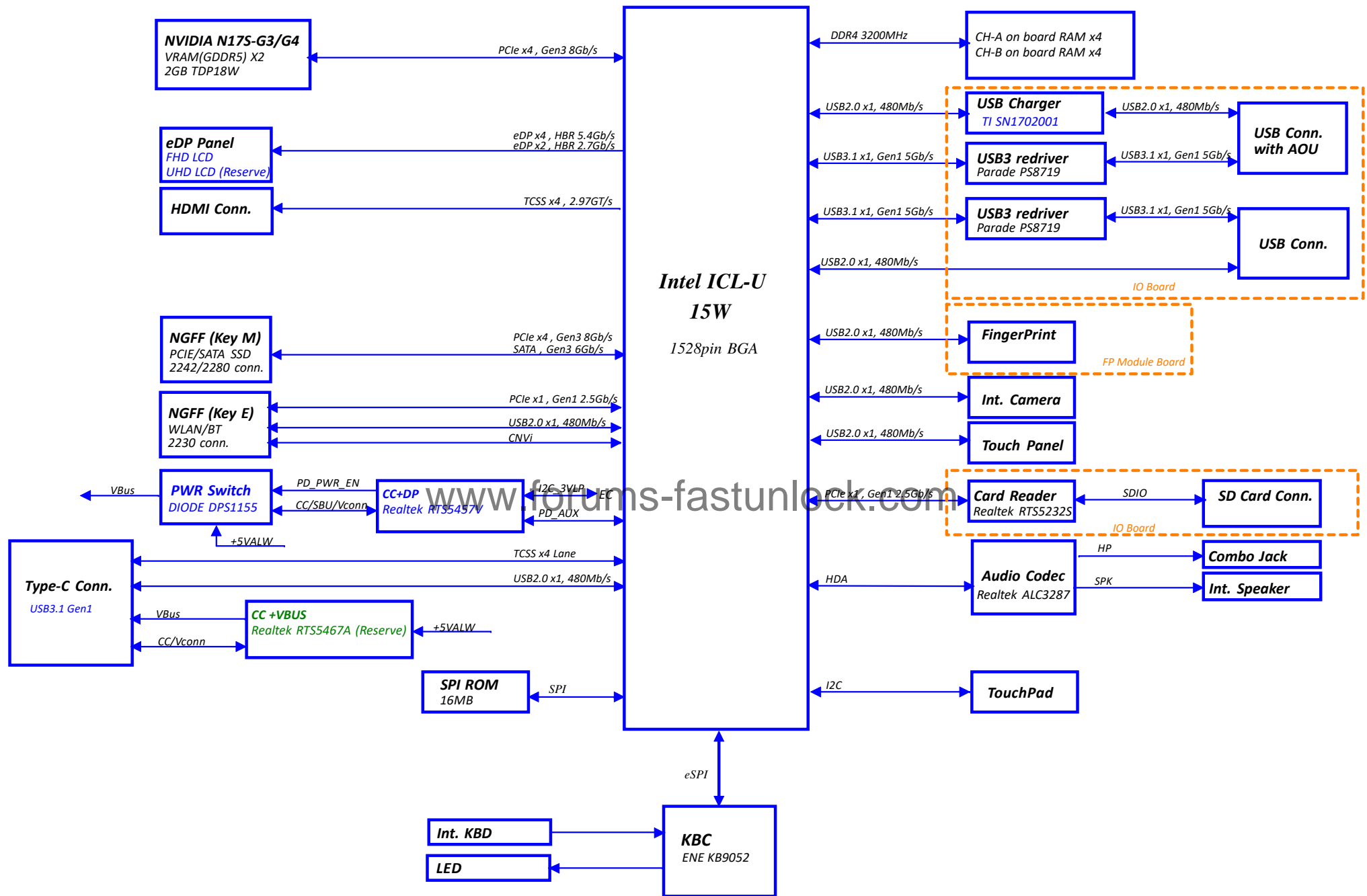
Intel Ice Lake-U Processor with DDR4 Memory Down

2019-08-22

LA-J551P

REV : 0 . 2

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Issued Date	2019/05/15	Deciphered Date	2020/05/15	Title Cover Page	
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Voltage Rails

power plane	+12.6VB	+5VALW +3VALW +1.8VALW	+1.2V +2.5V	+5VS +3VS +1.8VS +0.6VS +1.05V_VCCST +1.05VS_VCCSTG +VCCIN +VCCIN_AUX +1.8VS_DGPU +1.8VS_DGPU_AON +VGA_CORE +1.0VS_DGPU +1.35VS_VRAM
State				
S0	O	O	O	O
S3	O	O	O	X
S5 S4/AC	O	O	X	X
S5 S4/ Battery only	O	X	X	X
S5 S4/AC & Battery don't exist	X	X	X	X

BOM Structure Table

Item	BOM Structure
GPU N17S-G0/G2	DIS@ UMA@
Debug	DCI@ SDP@
Memory Down - SDF Package	SDP_CHB@
Memory Down - DDP Package	DDP@ DDP_CHB@
Only CHB Memory Down	CHB@
Intel CNVi	CNVi@
Keyboard BackLight	KBL@
EMI Category	EMI@
ESD Category	ESD@
RF Category	RF@
Normal FP Device	FP@
SLIM_FP	SLIM_FP@
+12V FAN CAP	
+5V FAN CAP	
CPU MIC (Reserve)	Array_MIC@ Single_MIC@ SOIX@
Modern standby	NOS0IX@
Project select	
DDR4 Memory Down CHB	CHB@
GPU GC6 Mode	GC6@ NOGC6@
Touch Screen Power	TS@
EC9052Q C Version	EC9052_C@
Option Bypass USB Charger	NON_AOU@
RMT tool test	RMT@ QSQS_R1@ QSQP_R1@ QSQV_R1@ QSVV_R1@ QSQW_R1@
CPU select	

Item	BOM Structure
DGPU chip select	N17S_G0_R1@ N17S_G0_R3@ N17S_G2_R1@ N17S_G2_R3@
VRAM chip select	VRAM_M2G_R1@ VRAM_M2G_R3@ VRAM_H2G_R1@ VRAM_H2G_R3@ VRAM_S2G_R1@ VRAM_S2G_R3@

USB 2.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	USB2/3 Port (Type-C)
4	Touch Screen
5	
6	Camera
7	Fingrt Print
8	
9	
10	NGFF WLAN+BT

TCP Port Table

Port	Lane
0	TYPE C (PD + CC)
1	HDMI
2	
3	

USB 3.0 Port Table

Port	External USB Port
1	USB2/3 Port (IO - 1)
2	USB2/3 Port (IO - 2)
3	
4	
5	
6	

PCIe Port Table

Port	Lane	
1		
2		
3		
4	0	
5	0	
6	1	GPU
7	2	
8	3	
9	1	CardReader
10	0	NGFF WLAN+BT
11		
12	0	
13	3	SSD
14	2	
15	1	
16	0	

SATA Port Table

Port	
0	
1A	
1B	SSD

EC SM Bus1 address EC SM Bus2 address

Device	Address	Device	Address
Smart Battery	0001 011x 16h	Thermal Sensor (F75305M)	1001_101xb 9Ah
Charger (ISL88739A)	0001 001x 12h	Thermal Sensor (F75397M)	1001_100xb 98h

PCH SM Bus address GPU SM Bus address

Device	Address	Device	Address
DDR_JDIMM1	1010 010x A4h	Internal thermal sensor	1001 111x 9Eh
Touch_Pad			

SMBUS Control Table

	SOURCE	SOC	BATT	CHARGER	KB9052	SODIMM	Thermal Sensor	DGPU
EC_SMB_CK1	KB9052	X	V	V	X	X	X	X
EC_SMB_DA1	+3VL		+3VALW	+19V_VIN				
EC_SMB_CK2	KB9052	V	X	X	X	X	V	V
EC_SMB_DA2	+3VS						+3VS	+3VS
EC_SMB_CK4	KB9052	X	X	X	X	X	X	X
EC_SMB_DA4	+3VS							
SOC_SMBCLK	SOC	X	X	X	X	V	X	X
SOC_SMBDATA	+3VS							
SOC_SML0CLK	SOC	X	X	X	X	X	X	X
SOC_SML0DATA	+3VS							

STATE	SIGNAL	SLP_S1#	SLP_S3#	SLP_S4#	SLP_S5#	+VALW	+V	+VS	Clock
Full ON		HIGH	HIGH	HIGH	HIGH	ON	ON	ON	ON
S1(Power On Suspend)		LOW	HIGH	HIGH	HIGH	ON	ON	ON	LOW
S3(Suspend to RAM)		LOW	LOW	HIGH	HIGH	ON	ON	OFF	OFF
S4(Suspend to Disk)		LOW	LOW	LOW	HIGH	ON	OFF	OFF	OFF
S5(Soft OFF)		LOW	LOW	LOW	LOW	ON	OFF	OFF	OFF

VRAM

ZZZ12 X76_H16G_2CH_2666@ X76 HYNIX 2GB X76843BL11	ZZZ12 X76_S2G_@ X76 SAMSUNG 2GB X76843BL12	ZZZ13 X76_M2G_@ X76 MICRON 2GB X76843BL11
---	--	---

ON BOARD RAM X76

ZZZ16 X76_M4G_1CH_3200@ X76 MICRON 4GB SINGEL X76843BL10	ZZZ6 X76_H4G_1CH_2666@ X76 HYNIX 4GB SINGEL X76843BL04	ZZZ3 X76_S16G_2CH_2666@ X76 SAMSUNG 16GB DUAL X76843BL02
--	--	--

ICL-U CPU

UC1 QSQS_R1@ I7-1065GT SA0000C7B10	UC1 QSQP_R1@ I5-1034G1 SA0000CUC10	UC1 QSOV_R1@ I5-1035G1 SA0000C7B10	UC1 QSVV_R1@ I3-1005G1 SA0000CVC010	UC1 QSQW_R1@ I3-1005G1 SA0000C7D10
--	--	--	---	--

ZZZ16 X76_M4G_1CH_3200@ X76 MICRON 4GB SINGEL X76843BL10	ZZZ6 X76_H4G_1CH_2666@ X76 HYNIX 4GB SINGEL X76843BL04	ZZZ3 X76_S16G_1CH_2666@ X76 SAMSUNG 4GB SINGEL X76843BL02
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DGPU

R1 UV1 SA0000CC940 N17S_G0_R1@ N17S-G2	UV1 SA0000CCB30 N17S_G2_R1@ N17S-G2
R3 UV1 SA0000CC910 N17S_G0_R3@ N17S-G0	UV1 SA0000CCB10 N17S_G2_R3@ N17S-G2

ZZ6 X76_M8G_2CH_3200@ X76 MICRON 8GB DUAL X76843BL09	ZZZ6 X76_H8G_2CH_2666@ X76 HYNIX 8GB DUAL X76843BL03	ZZZ1 X76_S8G_2CH_2666@ X76 SAMSUNG 8GB DUAL X76843BL01
--	--	--

PCB PN

ZZZ PCB FL535 LA-H105P DN601LE000

X4E

ZZZ14 X4E_DIS@ X4E S550-ICL DIS X4EA7Y3BL01	ZZZ14 X4E_UMA@ X4E S550-ICL UMA X4EA7Y3BL02
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The diagram illustrates a complex power distribution network (PDN) for a system. It shows the flow of power from various input rails (VR / Load SW) through various power management ICs (PMICs, LDOs, DC-DC converters, and load switches) to various output rails (Power Rail Name).

Input Rails (VR / Load SW):

- +19VB
- +12V
- +5V
- +3V
- +1.35V
- +1.05V
- +1.8V
- +1.0V
- +1.8V
- +1.8V
- +1.8V

Power Rail Name:

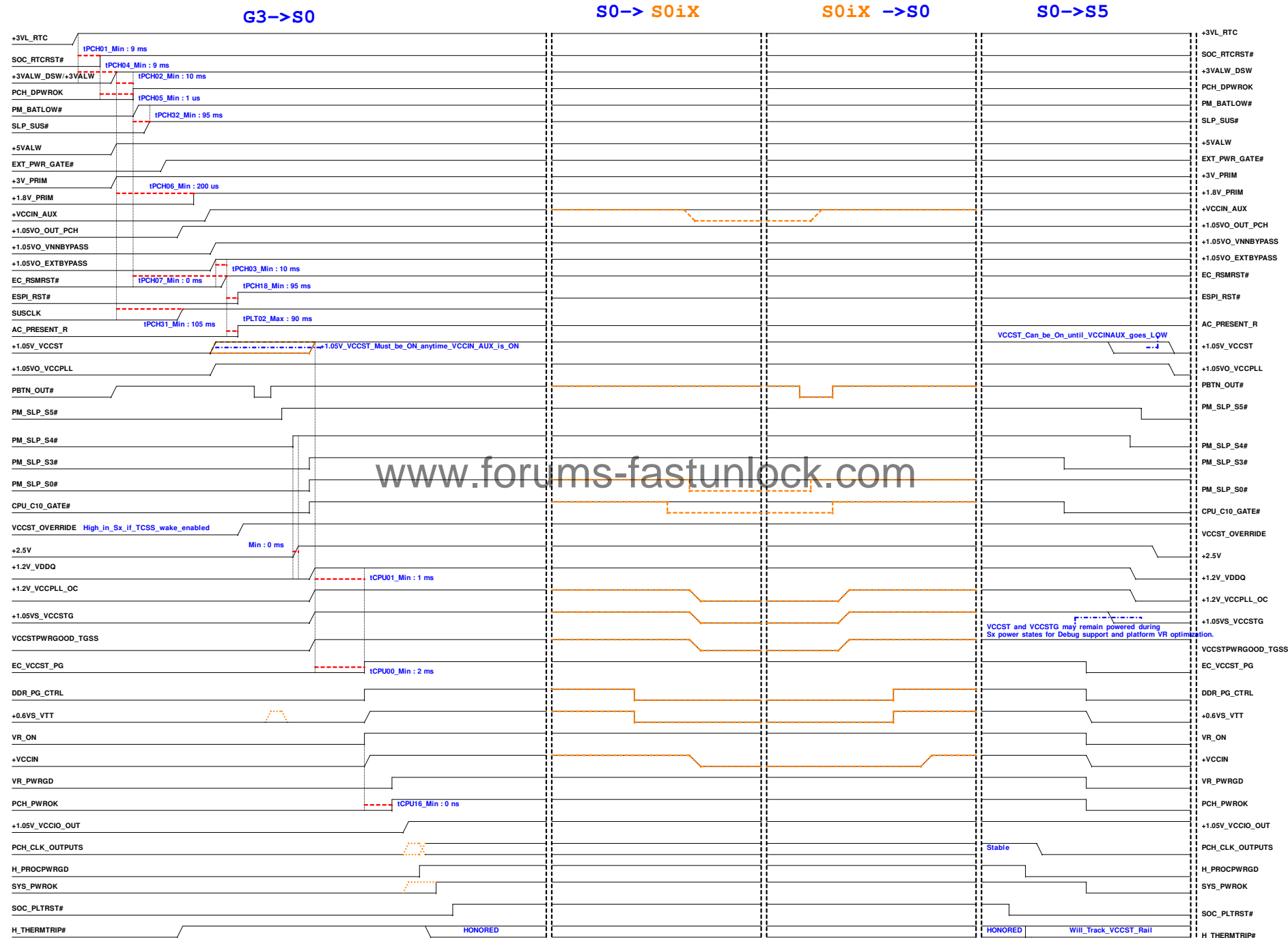
- +VCCIN
- +VCCIN_AUX
- +1.2V
- +0.6V
- +5V
- +3V
- +1.35V
- +1.05V
- +1.8V
- +1.0V
- +1.8V
- +1.8V
- +1.8V

Key Components and Connections:

- PUM1 (RT8207PGQW(LDO))** provides +1.2V and +0.6V.
- PU301 (RT657SDGQW(Dual LDOs))** provides +5V and +3V.
- PUW1 (SY8286RAC_QFN20(Load Switch))** provides +1.35V.
- Internal Power Rail VCC1P05** provides +1.05V.
- PUV1 (RT8816AGQW(VR))** provides +VGA_CORE.
- U42 (EM5209VF(Load Switch))** provides +1.2V.
- U13 (EM5209VF(Dual Load SW))** provides +5V and +3V.
- RC385 (0.0402 5%)** provides +3V.
- PU2501 (G9661MF11U(LDO))** provides +2.5V.
- PU1 (SY8032ABC(LDO))** provides +1.8V.
- PJ1801 (JUMP_43X79(@))** provides +1.8V.
- PU1803 (G9661MF11U(LDO))** provides +1.0V.
- PJ2 (JUMP_43X79(@))** provides +1.0V.
- RC311 (0.0402 5%)** provides +1.8V.
- U42 (EM5209VF(Load Switch))** provides +1.8V.
- U12 (TPS22961DNYS(Load Switch))** provides +1.8V.
- UV2 (EM5209VF(Dual Load SW))** provides +1.8V.

EN (Enable) Signals:

- EN: DRVON
- EN: 1.8V_PWRGD
- EN: SYSON
- EN: SUSP#
- EN: EC_ON
- EN: 1.35V_PWR_EN
- EN: VCCSTG_EN_LS
- EN: PCH_PWR_EN
- EN: SUSP#
- EN: PM_SLP_S3#
- EN: CPU_C10_GATE#
- EN: DGPU_MAIN_EN
- EN: DGPU_PWR_EN



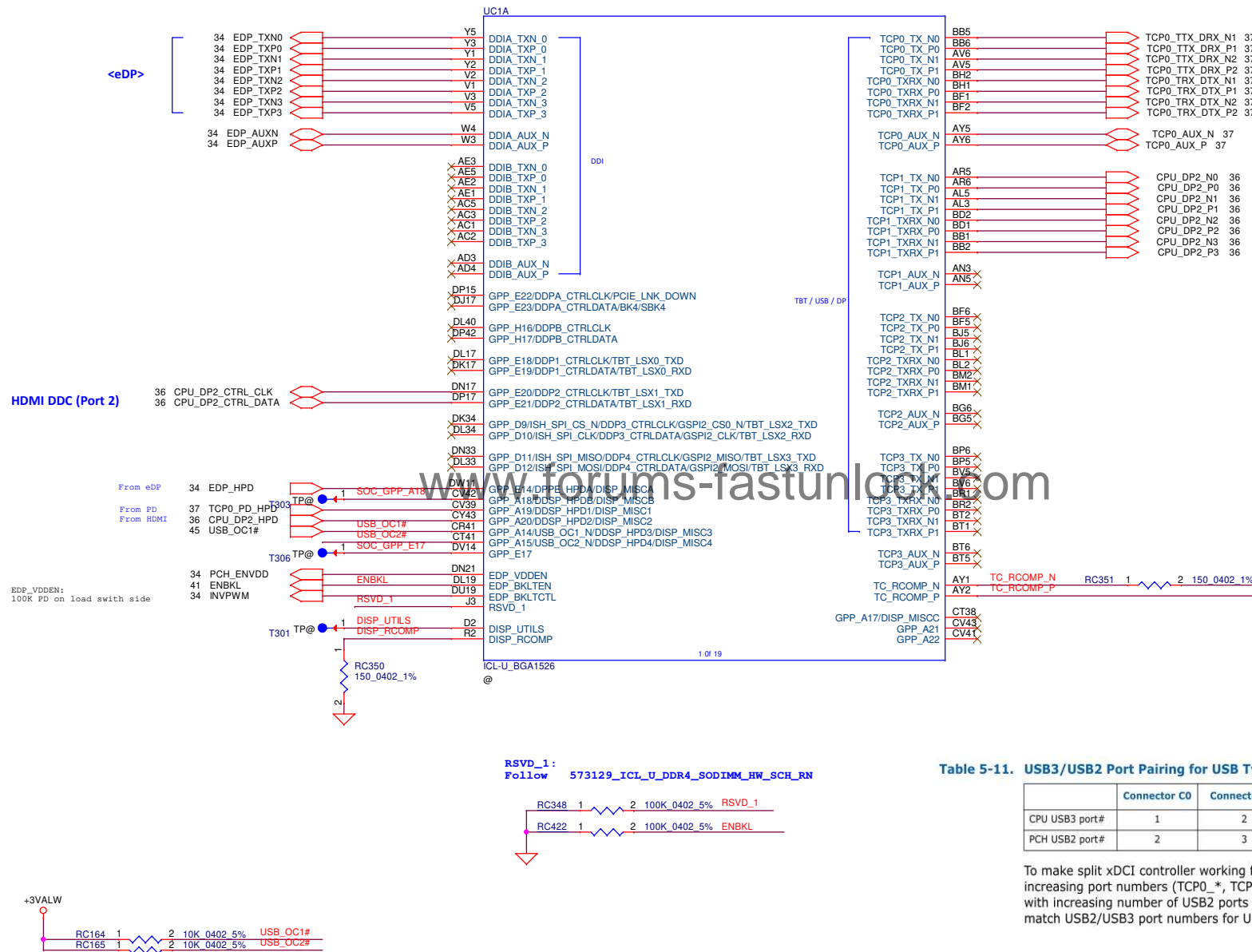


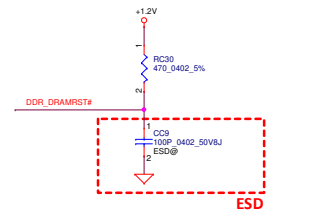
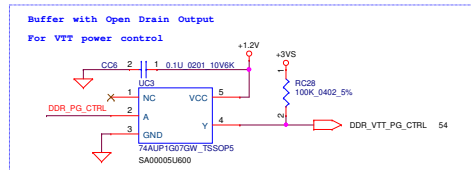
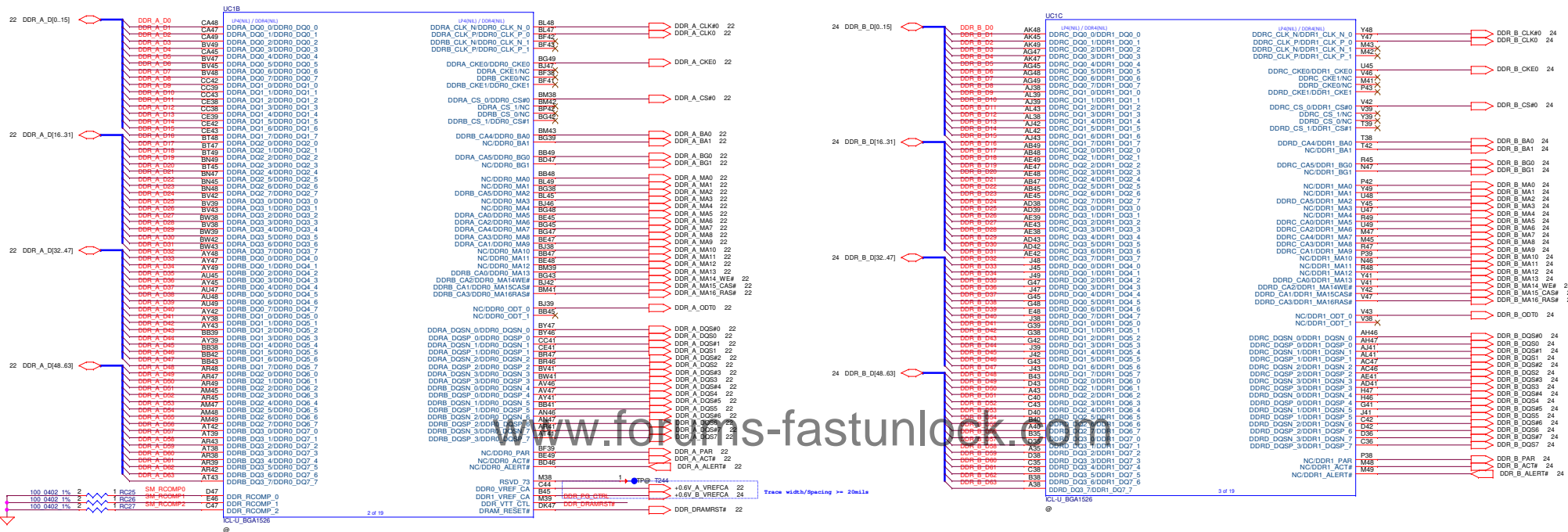
Table 5-11. USB3/USB2 Port Pairing for USB Type-C Connectors

	Connector C0	Connector C1	Connector C2	Connector C3
CPU USB3 port#	1	2	3	4
PCH USB2 port#	2	3	4	6

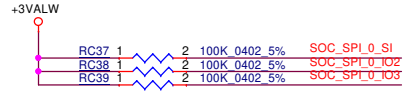
To make split xDCI controller working functionally for different USB-C connectors with increasing port numbers (TCP0_*, TCP1_*, TCP2_*, TCP3_*), recommended to pair with increasing number of USB2 ports from PCH. Simplest form of requirement is to match USB2/USB3 port numbers for USB-C connectors, but it is not strictly required.

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DDR4: Refer to 575034_ICL_U42_DDR4_T3_6L_Core_Schematics_Rev0p7



SPI ROM

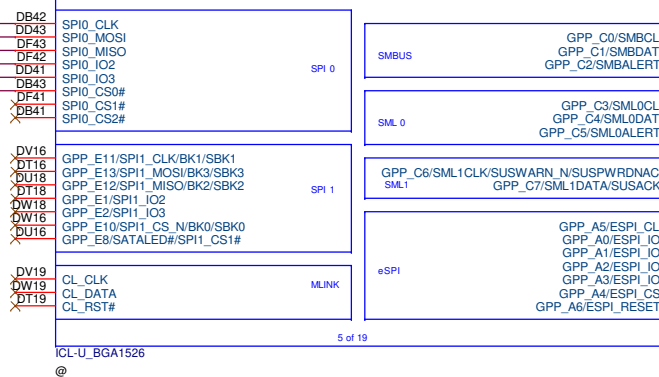


SOC_SPI_0_SO
BOOT HALT
NO INTERNAL PU/PD
HIGH: DISABLE
LOW: ENABLE

SOC_SPI_0_IO2
CONSENT STRAP
NO INTERNAL PU/PD
HIGH: DISABLE
LOW: ENABLE

SOC_SPI_0_IO3
A0 PERSONALITY STRAP
NO INTERNAL PU/PD
HIGH: DISABLE
LOW: ENABLE

UC1E



GPP_C2
TLS CONFIDENTIALITY
INTERNAL PD 20K
HIGH: TLS CONFIDENTIALITY ENABLE
LOW: TLS CONFIDENTIALITY DISABLE

SOC_SML0ALERT#
ESPI OR EC LESS
INTERNAL PD 20K
HIGH: ESPI DISABLE
LOW: ESPI ENABLE (Default)

SOC_GPP_C2 RC86 1 2 4.7K 0402 5%

SML1
(Link to GPU, EC, Thermal Sensor, PD)

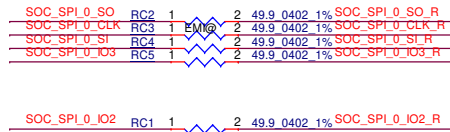
ESPI
Follow
572907_ICL_UY_PDG

SPI0_MOSI	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO2	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.
SPI0_IO3	Reserved	Rising edge of RSMRST#	External pull-up is required. Recommend 100K if pulled up to 3.3V or 75K if pulled up to 1.8V. This strap should sample HIGH. There should NOT be any on-board device driving it to opposite direction during strap sampling.

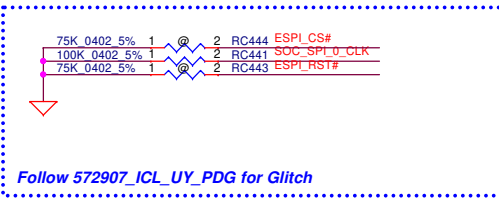
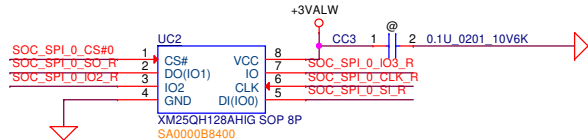
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close to SPI ROM

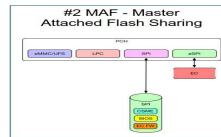
From SOC



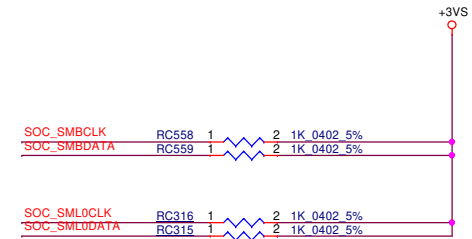
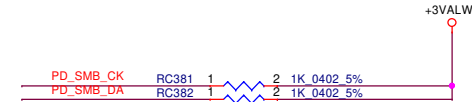
< SPI ROM - 16M >



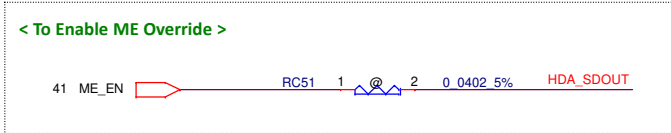
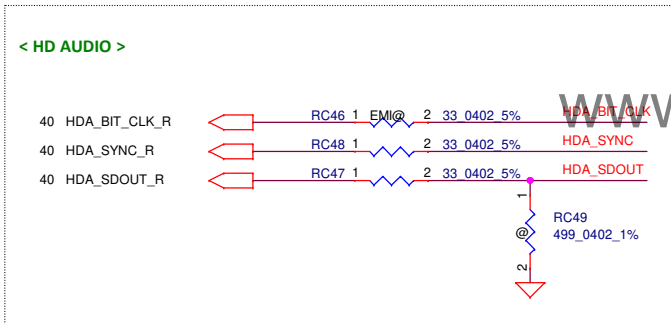
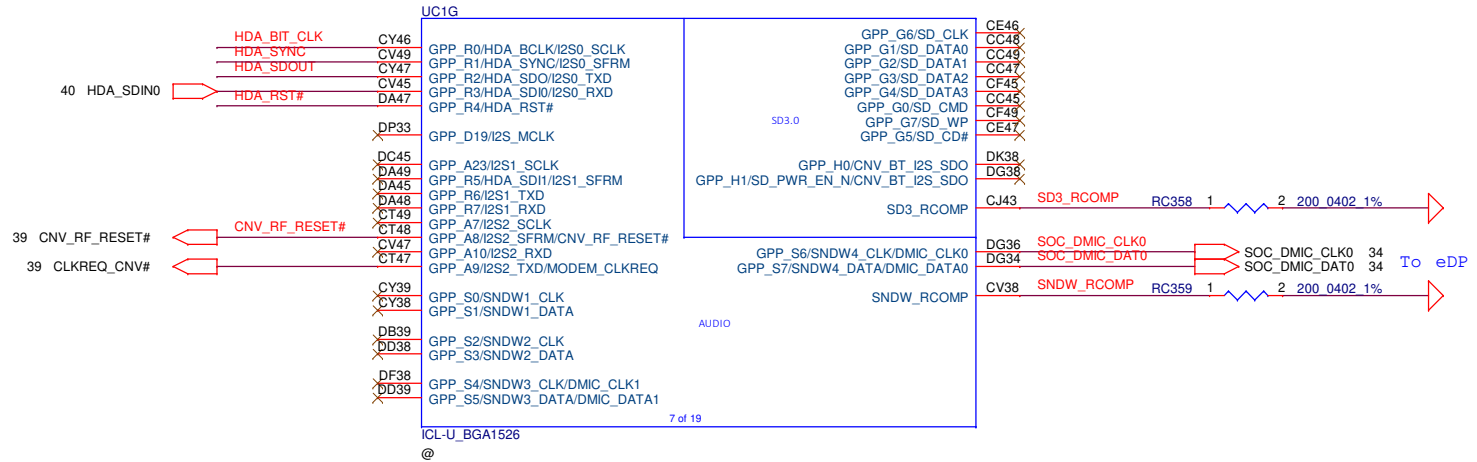
Follow 572907_ICL_UY_PDG for Glitch



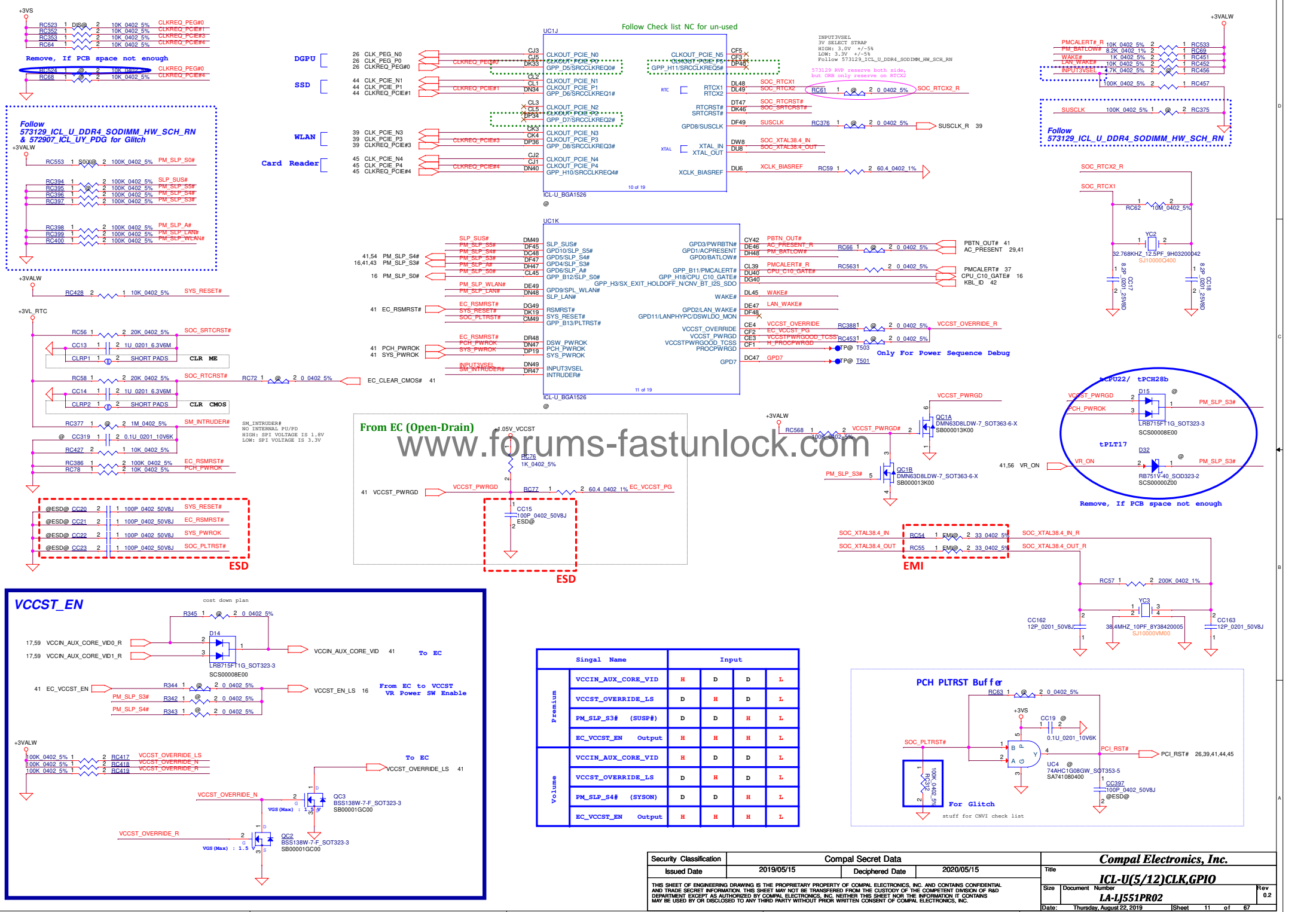
MAF - Master Attached Flash
Single SPI Flash attached to SPI Bus
EC FW access through eSPI Bus



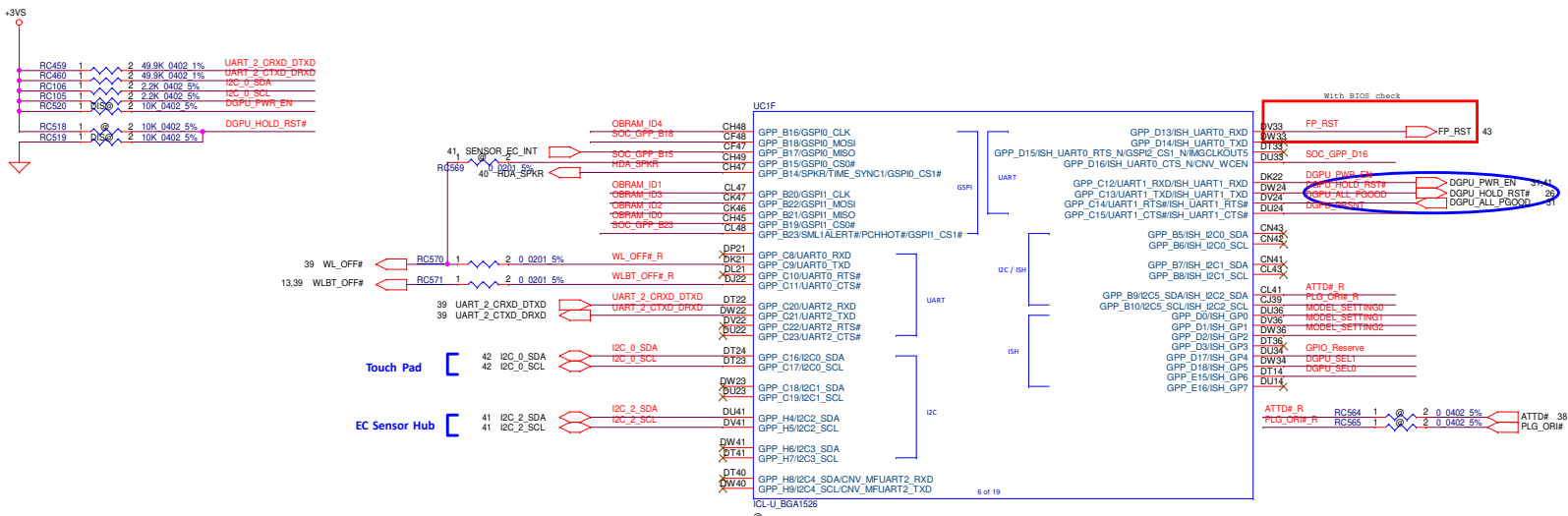
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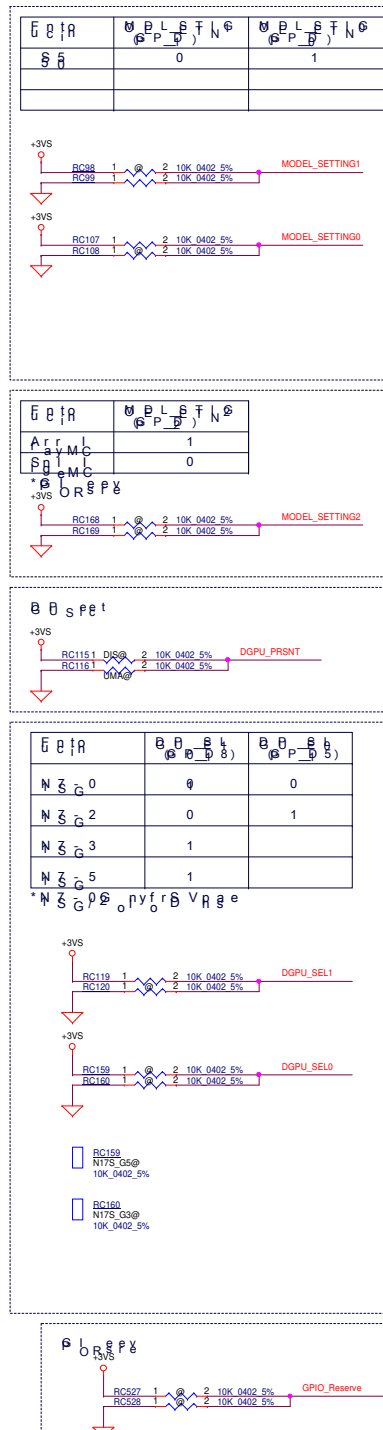
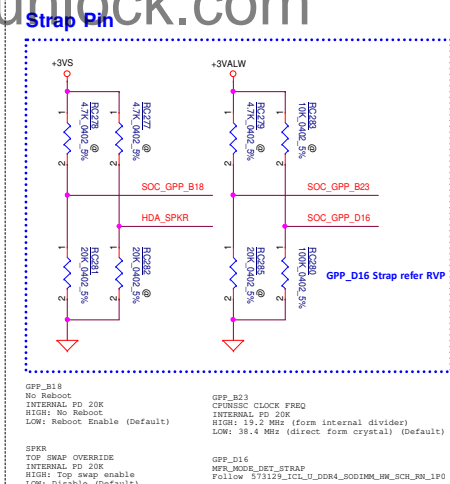
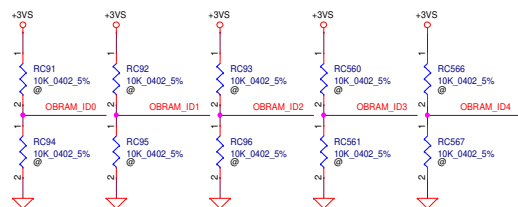


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Place the same side(TOP/BOT) with on board RAM IC

Capacity	Description	Part Number	Used Channel	OBRAM_ID4	OBRAM_ID3	OBRAM_ID2	OBRAM_ID1	OBRAM_ID0	X76 Number	DDR4 System total size
8Gb-2666	SS D4 K4A8G165WC-BCTD SDF	SA0000B6F00	1	0	0	0	0	0	X7684838L02	4GB
	HY D4 H5AN8G6NCIR-VKC SDF	A0000BMN00	1	0	0	0	0	1	X7684838L04	
16Gb-2666	SS D4 K4AAG165WA-BCTD SDF	SA0000CNO00	1	0	0	0	0	0	X7684838L06	8GB
	HY D4 H5ANAG6NCMR-VKC DDP	SA0000BZ100	1	0	0	0	0	1	X7684838L08	
8Gb-3200	SS D4 K4A8G165WC-BCWE SDF	SA0000CZ500	1	0	0	1	0	0	TBD	4GB
	HY D4 H5AN8G6NCIR-XNC SDF	SA0000CZ300	1	0	0	1	0	1	TBD	
16Gb-3200	MC D4 MT40A512M16TB-062E:J SDF	SA0000CMS00	1	0	0	1	1	0	X7684838L10	8GB
	SS D4 K4AAG165WA-BCWE SDF	SA0000CZ200	1	0	0	1	1	1	TBD	
16Gb-3200	HY D4 H5ANAG6NCIR-XNC DDP	SA0000CZ100	1	0	1	0	0	0	TBD	8GB
	MC D4 MT40A1G16RC-062E:B SDF	SA0000CSR00	1	0	1	0	0	1	TBD	
8Gb-2666	SS D4 K4A8G165WC-BCTD SDF	SA0000B6F00	2	1	0	0	0	0	X7684838L01	8GB
	HY D4 H5AN8G6NCIR-VKC SDF	A0000BMN00	2	1	0	0	0	1	X7684838L03	
16Gb-2666	SS D4 K4AAG165WA-BCTD SDF	SA0000CNO00	2	1	0	0	1	0	X7684838L05	16GB
	HY D4 H5ANAG6NCMR-VKC DDP	SA0000BZ100	2	1	0	0	1	1	X7684838L07	
8Gb-3200	SS D4 K4A8G165WC-BCWE SDF	SA0000CZ500	2	1	0	1	0	0	TBD	8GB
	HY D4 H5AN8G6NCIR-XNC SDF	SA0000CZ300	2	1	0	1	0	1	TBD	
16Gb-3200	MC D4 MT40A512M16TB-062E:J SDF	SA0000CMS00	2	1	0	1	1	0	X7684838L09	16GB
	SS D4 K4AAG165WA-BCWE SDF	SA0000CZ200	2	1	0	1	1	1	TBD	
16Gb-3200	HY D4 H5ANAG6NCIR-XNC DDP	SA0000CZ100	2	1	1	0	0	0	TBD	16GB
	MC D4 MT40A1G16RC-062E:B SDF	SA0000CSR00	2	1	1	0	0	1	TBD	
16Gb-3200	MC D4 MT40A1G16KD-062E:E SDF	TBD	2	1	1	0	1	0	TBD	16GB
	MC D4 MT40A1G16KD-062E:E SDF	TBD	2	1	1	0	1	0	TBD	



SVID CLOCK

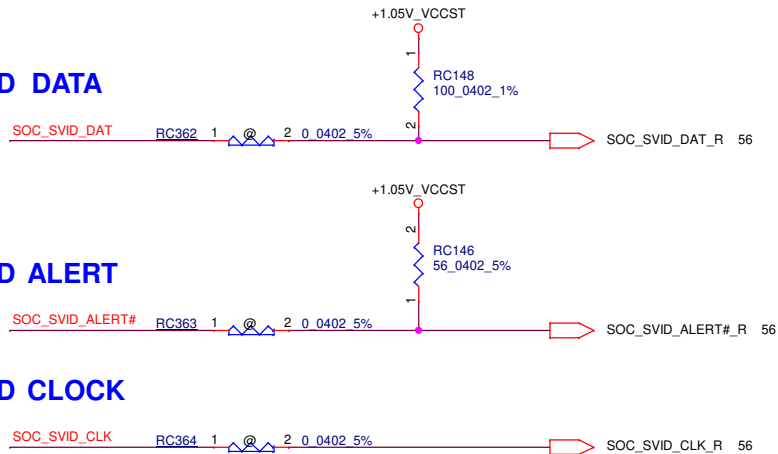


Figure 5-54. Routing Illustration for SVID Topology

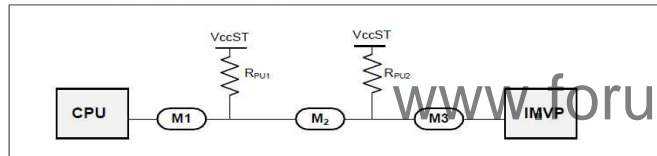
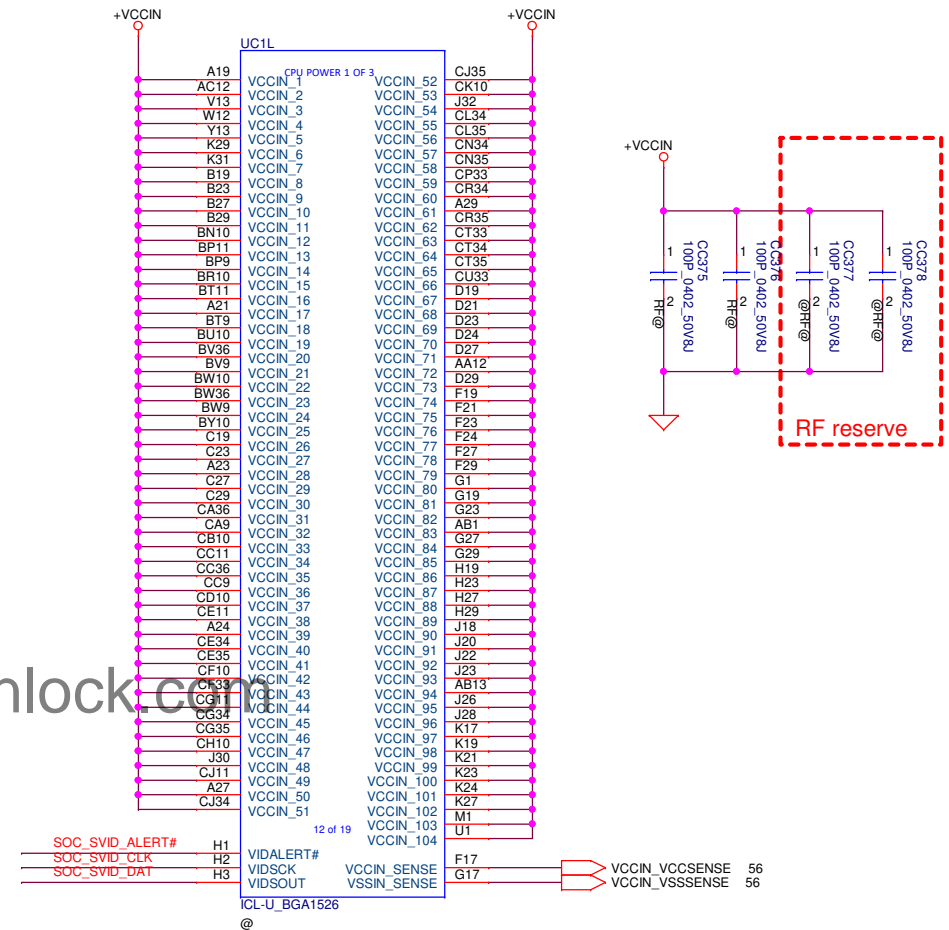


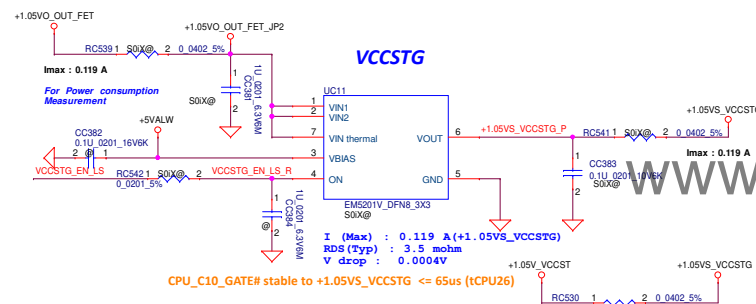
Figure above demonstrates Routing Illustration for SVID Topology, each trace from CPU to VR represents 3 signals: VIDSOUT, VIDSCK, VIDSALERT#.

Table 5-75. SVID Routing Guidelines

Segment	Tline Type	Reference	Via Count	Max Length, mm	
				Segment	Total
M1	MS/SL/DSL	VSS		75	530
M2	MS/SL/DSL	VSS		380	
M3	MS/SL/DSL	VSS		75	
Topology Guidelines					
SVID Signals		VIDSOUT, VIDSCK, VIDSALERT#			
VIDSOUT platform resistors		Rpu1=100Ω, Rpu2=100Ω			
VIDSCK platform resistors		Rpu1=Empty, Rpu2=45Ω			
VIDSALERT# platform resistors		Rpu1=56Ω, Rpu2=Empty			
Platform resistors tolerances		± 5%			
Route ordering		When routing at minimum spacing route Alert between Data and Clock			



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[illegible][illegible]

For Power consumption Measurement

UC14 MOSFET

VIN1
VIN2
VIN thermal
VBIAS
ON
GND

VOUT

EM5201V_DFN8_3X3
S01X@

RDS(Typ) : 3.5 mohm
V drop : 0.0004V

CC393
0.1u 0201_16VK
S01X@

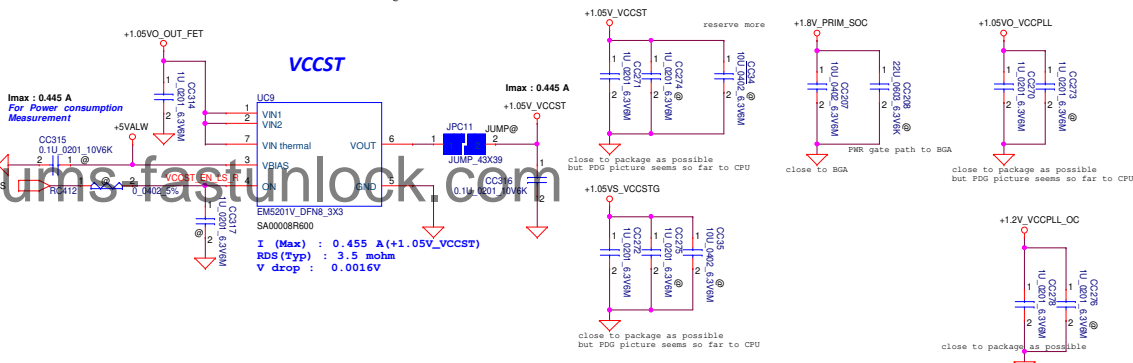
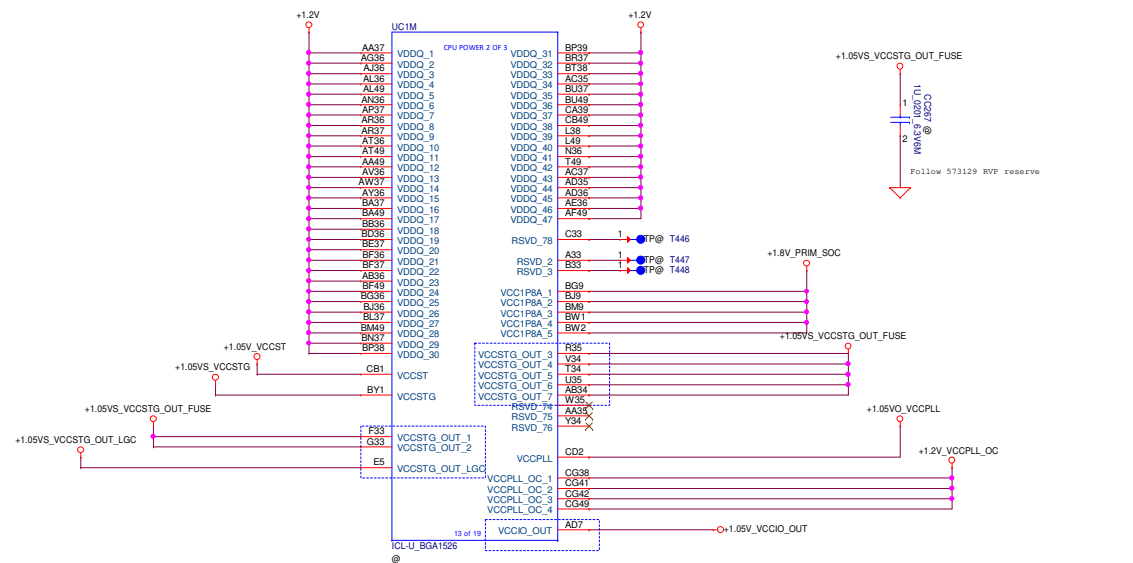
RC550 1 S01X@ 2 0.0402 5%

RC552 1 N050X@ 2 0.0603 5%

CC395
0.1u 0201_10VK
S01X@

+5VALW
+1.8V_VALW_P
+1.8V_PRIM_SOC
+1.8V_PRIM_SOC

Imax : 0.119 A
Imax : 0.7 A



The diagram shows a parallel circuit with three capacitors connected to a +1.2V supply and ground. The capacitors are labeled CC189, CC190, and CC191, each with a value of 220.0000 and a voltage rating of 6.3V66M. The capacitors are connected in parallel between the +1.2V supply and ground.

UC13

VN1

VN2

VN thermal

VBIAS

EM5201V_DFN5_3K3

VOUT

GND

+1.8VS

CC389 1u_0201_6.3V8M

CC391 0.1u_0201_16V6K

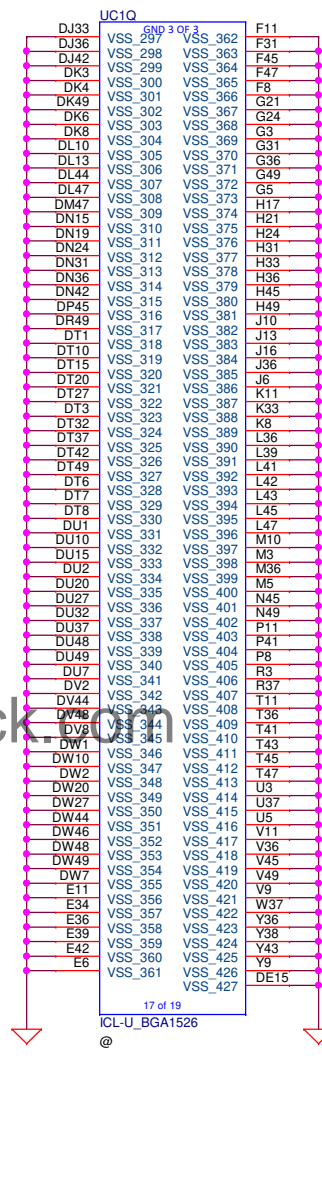
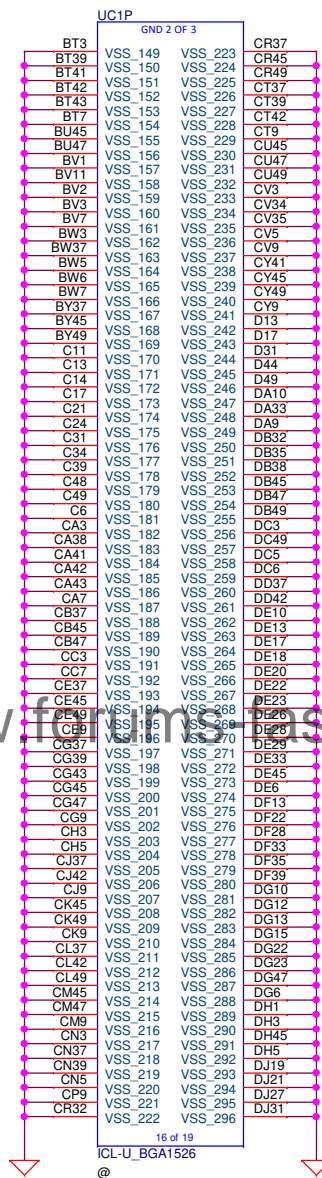
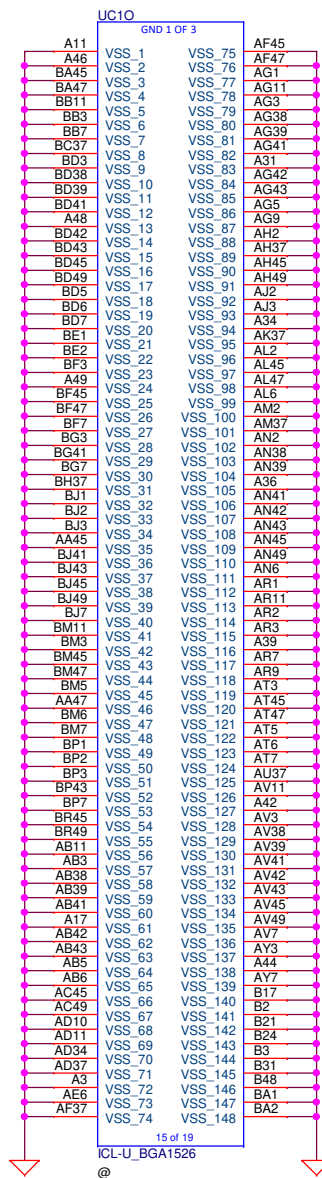
CC394 1u_0201_6.3V8M

CC392 0.1u_0201_10V6K

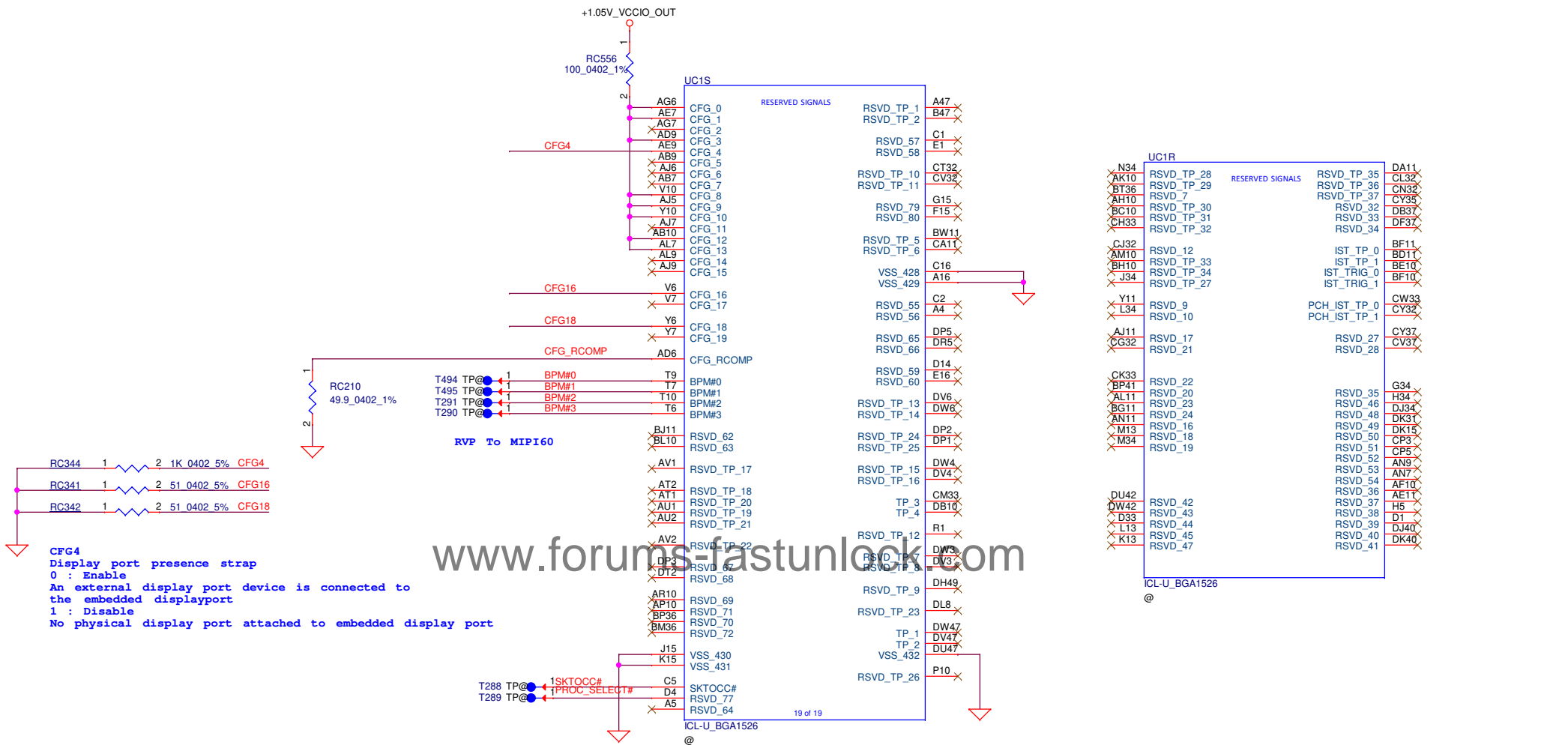
RDS (Typ) : 3.5 mohm

V drop : 0.0004V

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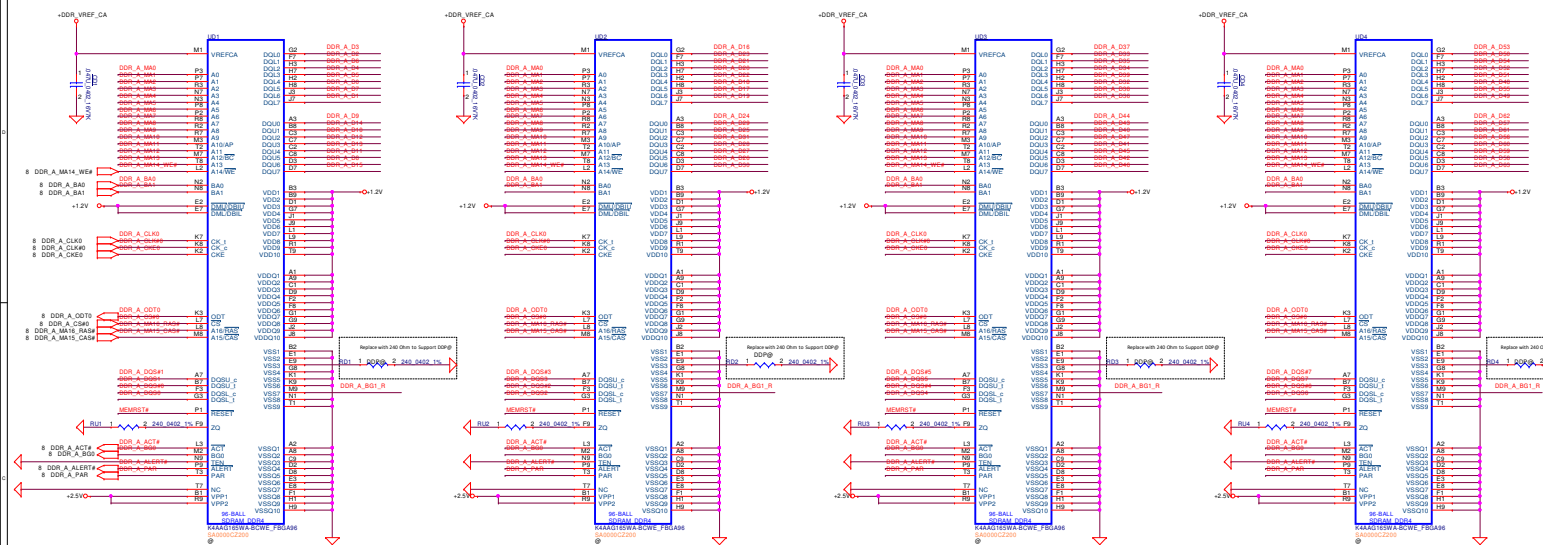
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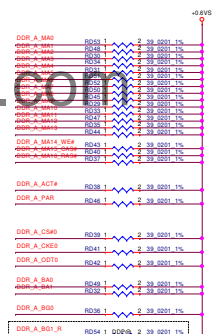
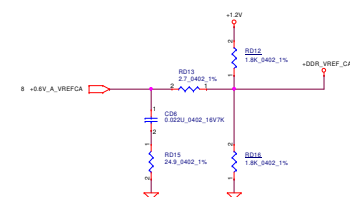
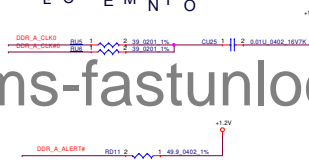
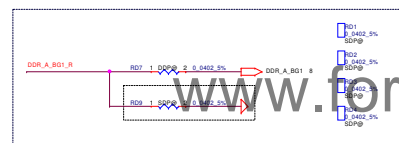
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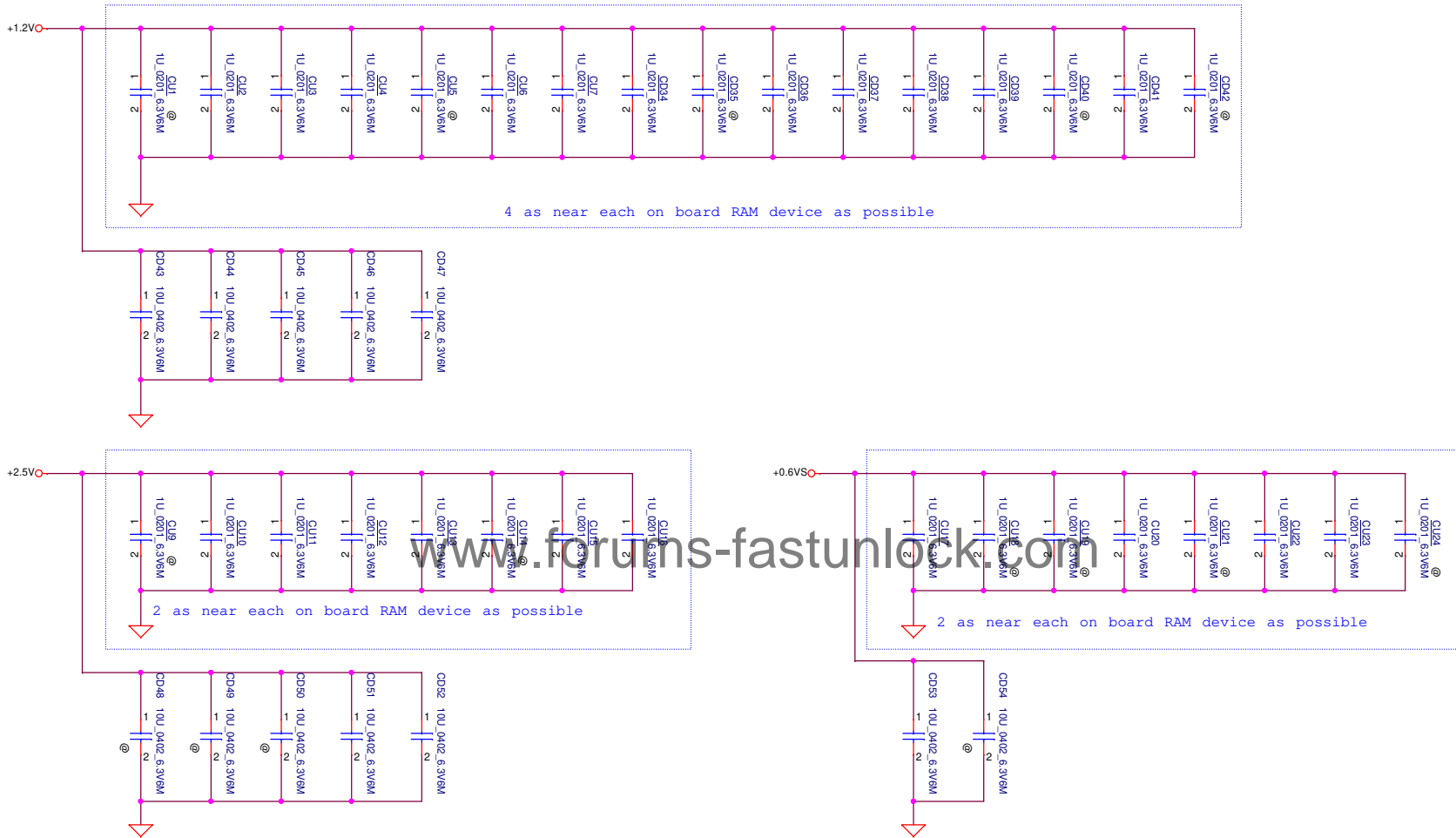
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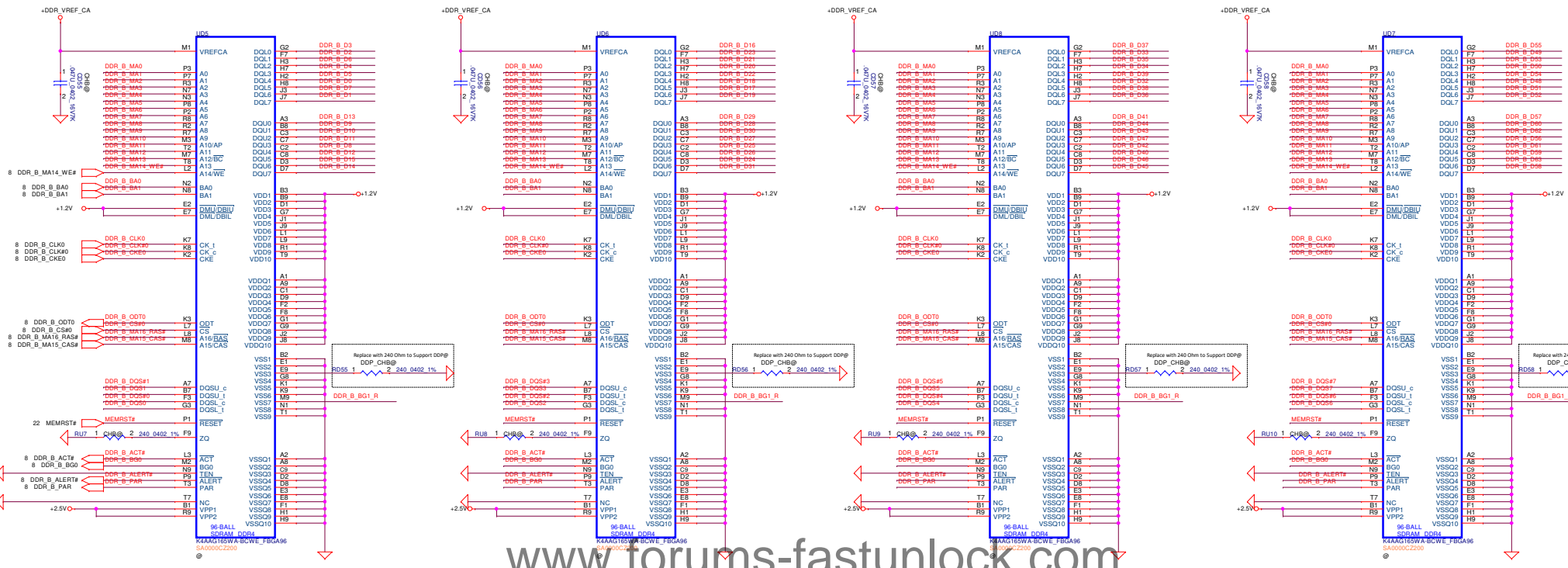


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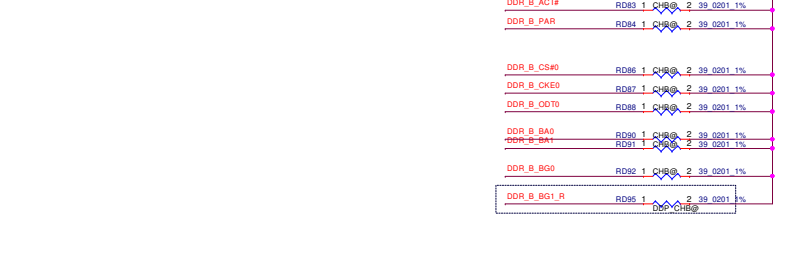
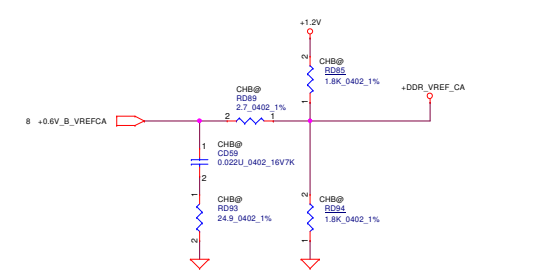
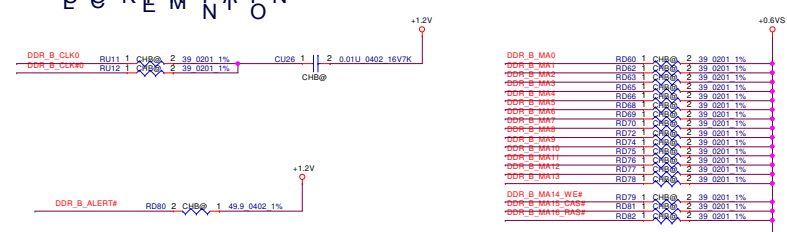
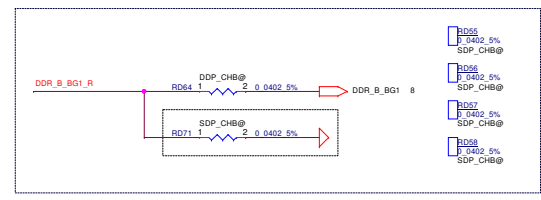
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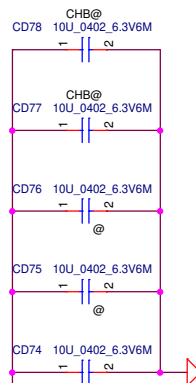
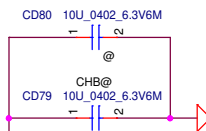
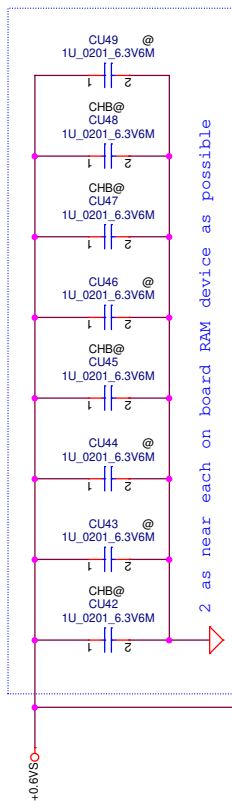
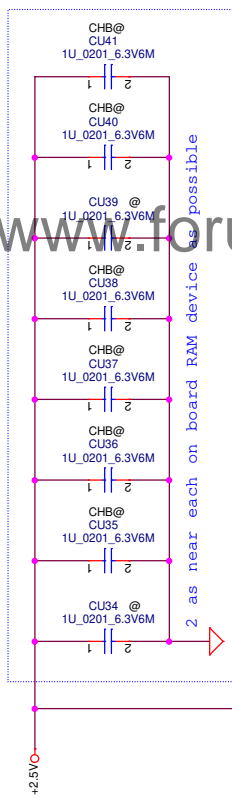
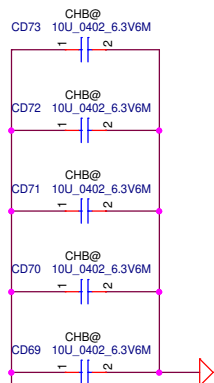
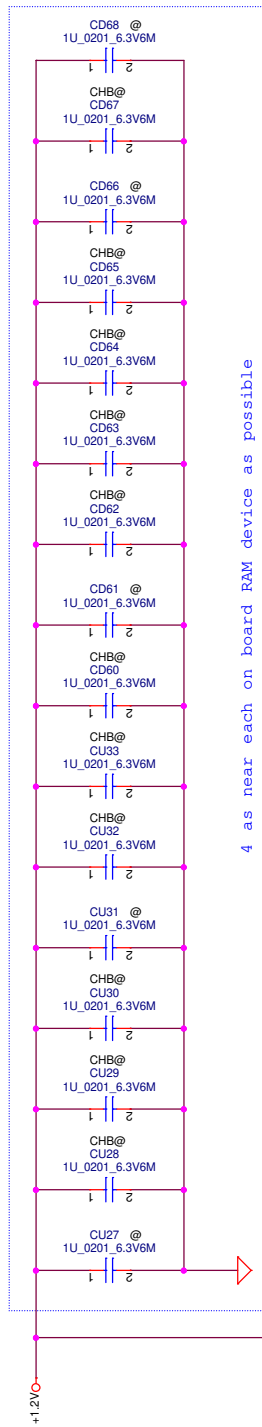


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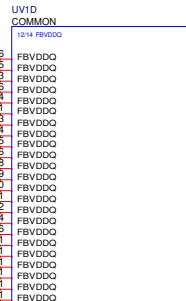
GPU Package Type	Capacitor Type	Footprint	Population	Location
GB26-64/ GB2-64	1.0 μ F X65	0402	1	Under GPU
	.47 μ F X65	0603	1	Near GPU
	10 μ F XSR	0805	1	Midway between GPU and Power Supply
	22 μ F XSR	0805	1	Midway between GPU and Power Supply

Table 6. PEX Core and IO Supply Decoupling and Filtering

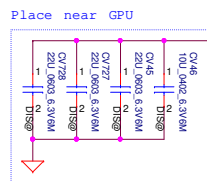
GPU	Capacitor Type	Footprint	Population		Location	
			N16	N17		
N16 PEX_IOVDD (N17 PEX_DVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 μ F	X65	D402	1	1	Under GPU
	4.7 μ F	X65	D603	0	1	Under GPU
	4.7 μ F	X65	D603	1	2	Near GPU
	10 μ F	X65	0805	0	2	Midway between GPU and Power Supply
	22 μ F	X65	0805	0	1	Midway between GPU and Power Supply
N16 PEX_IOVDDQ (N17 PEX_HVDD) Supply Rail						
GB2B-64, GB2C-64	1.0 μ F	X65	D402	1	4	Under GPU
	4.7 μ F	X65	D603	1	2	Near GPU
	10 μ F	X65	0805LP	1	2	Midway between GPU and Power Supply
	22 μ F	X65	0805LP	1	1	Midway between GPU and Power Supply

Table 7. PEX PLLs Decoupling and Filtering

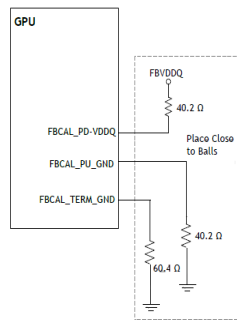
GPU	Capacitor Type	Footprint	Population N16	N17	Location
PEX_PLLVDD Supply Rail					
GB2B-64	0.1 μ F X7R	0402	1	N/A	Under GPU
	1.0 μ F X5R	0603	2	N/A	Near GPU
	4.7 μ F X5R	0805	1	N/A	Near GPU
PEX_VDDX_VV3 Supply Rail					
GB2B-64	4.7 μ F X5R	0603	2	N/A	Near GPU
Capacitor Type		Footprint	Population N16	N17	Location
EXP_PLL_VHDD Supply Rail					
GB2B-64	0.1 μ F X7R	0402	1	1	Near GPU



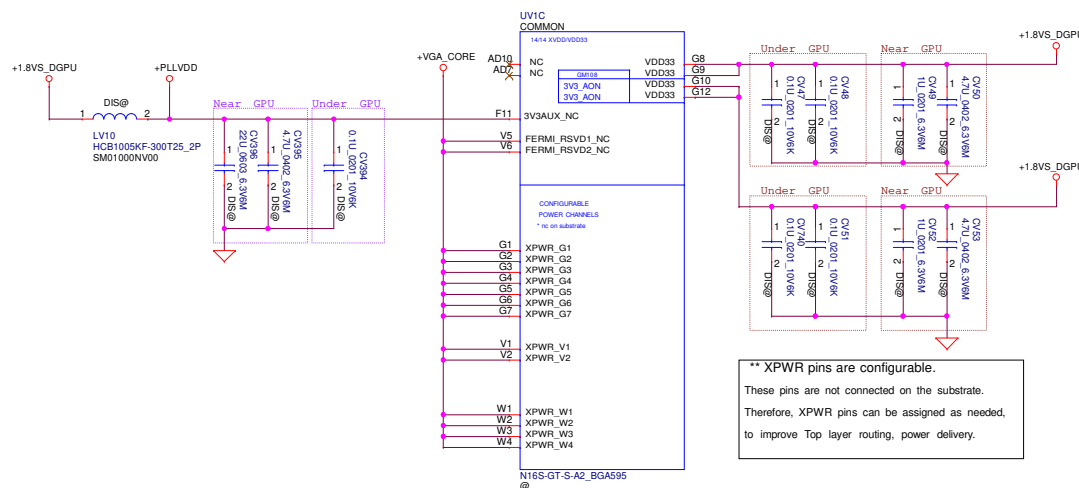
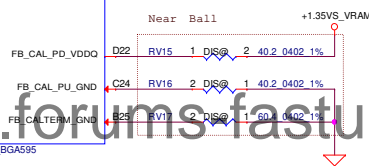
GPU	Capacitor Type		Population			
	Footprint		N16	N17	Location	
FBVDDQ Supply Rail for GDDR5						
GR28-64, GR2C-64	0.1 μ F	X7R	0402	2	0	Under GPU
	1 μ F	X7R	0603	2	8	Under GPU
	4.7 μ F	X6S	0603	2	0	Under GPU
	10 μ F	X6S	0603	0	2	Under GPU
	10 μ F	X6S	0603	1	1	Near GPU
	22 μ F	X6S	0603W	1	3	Near GPU



GPU Package Type	Capacitor Type	Footprint	Population	Location	
GB25-64	0.1 μ F	X7R 0402	2	2	Under GPU
GB2-64	1 μ F	X7R 0603	2	2	Under GPU
GDDR5	4.7 μ F	X6S 0603	2	2	Under GPU
	10 μ F	X5R 0805	1	1	Near GPU
	22 μ F	X5R 0805	1	1	Near GPU



Note: Use only 1% resistors for driver calibration

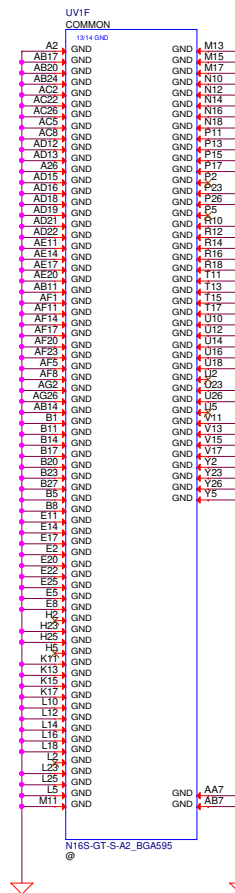


NC (N17: GPCPLL_AVDD) Supply Rail						
GB2C-64	0.1 μ F	X7R	0402	N/A	1	Under GPU
	4.7 μ F	X6S	0603	N/A	1	Near GPU
	22 μ F	X6S	0805	N/A	1	Near GPU
	Bead Type					
	L=30 Ω (ESR=0.010 Ω)	0603	N/A	1	Near GPU	

The diagram shows the pinout for the N165-GT-S-A2 BGA598 package. A red line indicates the voltage level for each pin, categorized as follows:

- VGA CORE**: Pins K10 through V18.
- Voltage by GPU SKU**: Pins M10 through V18.
- COMMON**: Pins U11 through U13.
- 1V14 NVDD**: Pins V14 through V18.

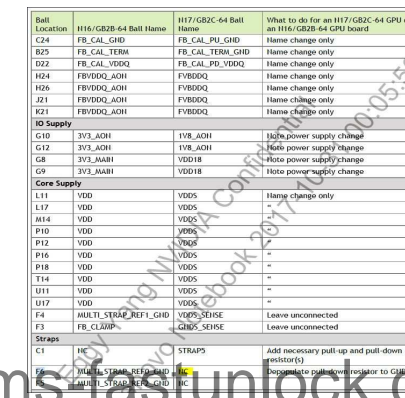
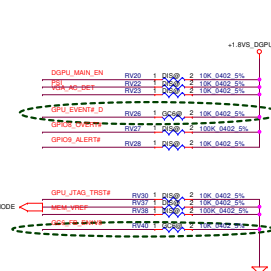
Pin Label	Voltage Level
K10	VDD
K12	VDD
K14	VDD
K16	VDD
K18	VDD
L11	VDD
L13	VDD
L15	VDD
L17	VDD
M10	VDD
M12	VDD
M14	VDD
M16	VDD
M18	VDD
N11	VDD
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R13	VDD
R15	VDD
R17	VDD
T10	VDD
T12	VDD
T14	VDD
T16	VDD
T18	VDD
U11	VDD
U13	VDD
U15	VDD
U17	VDD
V10	VDD
V12	VDD
V14	VDD
V16	VDD
V18	VDD



GPU Package	Rail	Capacitor Type		Footprint		Population	Location
GB2-64	3V3_MAIN	0.1 μ F	X6S	0402	2	2	Under GPU
GB2B-64		1 μ F	X5R	0603	1	1	Near GPU
GB4B-128		4.7 μ F	X5R	0603	1	1	Near GPU
GB3B-256							
GB2-64	3V3_AQN	0.1 μ F	X6S	0402	1	1	Under GPU
GB2B-64		1 μ F	X5R	0603	1	1	Near GPU
GB4B-128		4.7 μ F	X5R	0603	1	1	Near GPU
GB3B-256							

Note: This table is for non-SLI mode. For SLI mode, please refer to the MIO Decoupling table.

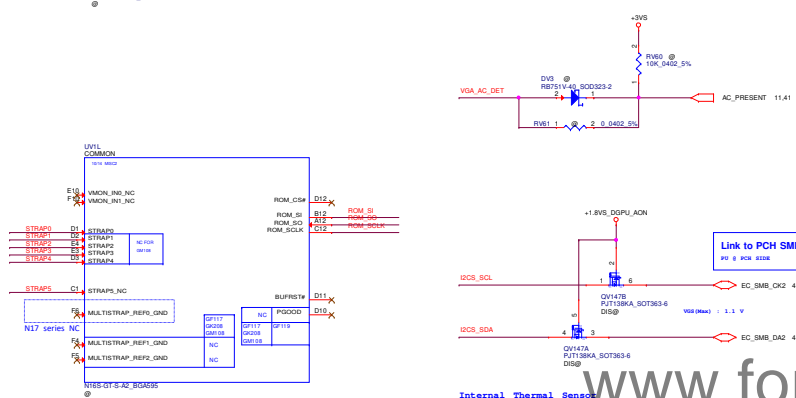
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Do not route unused I²C signals on the PCB in order to protect the GPU from outside ESD risk. If unused traces are routed, the signals should be pulled down to ground with 1.8 k Ω resistors.

N16x GPUs use FCS slave address 0x96h for NVIDIA internal testing. FC address 0x96h must not be used by other FC devices on the same bus as the GPU to avoid address conflict. The SMB_ALT_ADDR strap does not affect this 0x96h address. Refer to Chapter 15 (Straps) for a list of useful FCS Slave addresses can be used with SMB_ALT_ADDR strapping.

The internal thermal sensor can be accessed through the PCS interface as described in the FDC chapter. This interface is compliant with the System Management Bus (SMBus) Specification (Version 2.0). The interface supports PEC and SMBus Timeout as well as Read Byte and Read Byte with PEC. Writes to the internal thermal sensor registers through the FCS interface by the system is not supported. The default port address to access the internal thermal sensor over the FCS is 0x9E. Table 16-1 describes the byte-wise register accessible through the FCS interface.



GPIO Number	GPIO Name	I/O	Functional Description	IO Requirement
GPIO0	GCA_FBI_01	I	FBI Data for GCS 2.0, Open Source memory output for FBI	IO pull-up to V _{3T3_A01}
GPIO1	MEM_VIO_01	I	Memory output for FBI	IO pull-up to V _{3T3_A01} to set the FBPRG0 bit voltage
GPIO2	LOD_R_PWM	O	Power Backlight PWM Brightness Control	IO pull-up to V _{3T3_A01}
GPIO3	LOD_R_PWM_Enable	O	Power Backlight Enable	IO pull-up to V _{3T3_A01}
GPIO4	LOD_BLEH	O	Power Backlight Enable	IO pull-up to V _{3T3_A01}
GPIO5	V3T3_MAH_01	I	Power Backlight sequencing for GCS 2.0, Open Source	IO pull-up to V _{3T3_A01}
GPIO6	V3T3_VIO_01	I	Video I/O signal for GCS 2.0	IO pull-up to V _{3T3_A01}
GPIO7	DeviceID	I	30 Vision I/O signal	IO pull-up to V _{3T3_A01}
GPIO8	IO_VIO_RST_A01	I	Active Low I/O Reset control output	IO pull-up to V _{3T3_A01} unless actively driven
GPIO9	Thermal_ALERT	O	System Active Thermal Alert, Open Drain	IO pull-up to V _{3T3_A01}
GPIO10	MEM_VIO_02_CTL	I	Memory output for FBI	IO pull-up to V _{3T3_A01}
GPIO11	PWM_VIO	O	Power Backlight PWM control signal	IO pull-up to V _{3T3_A01}
GPIO12	PWR_LEVEL	I	IO-Beeper detect or power supply regulator input	IO pull-up to V _{3T3_A01}
GPIO13	PSI	I	Power Shedding	IO pull-up to V _{3T3_A01} to enable
GPIO14	HPD_A	I	Hot Plug Detect for HPFA used as DisplayPort [®] for HPFA when used as DisplayPort	See Figure 12-1
GPIO15	HPD_C	I	Hot Plug Detect for HPFA when used as DisplayPort [®] for HPFA when used as DisplayPort	See Figure 12-1
GPIO16	FRAME_LOC0A	I	Active Low Frame Lock, Open Drain	IO pull-up to V _{3T3_A01} , not available for G82B-64
GPIO17	D	O	Hot Plug Detect for HPFA	See Figure 12-1
GPIO18	HPD_C	I	Hot Plug Detect for HPFA	See Figure 12-1
GPIO19	HPD_C	I	Hot Plug Detect for HPFA	See Figure 12-1
GPIO20	HPD_C	I	Hot Plug Detect for HPFA	See Figure 12-1
GPIO21	HPD_C	I	Hot Plug Detect for HPFA	See Figure 12-1
GPIO22	Reserved			
GPIO23	GPI_V3T3_HOTEN	I	GPIO Pin reset control, Open Drain	IO pull-up to V _{3T3_A01}
GPIO24	OverTemp	O	Catapultic Over Temperature	IO pull-up to V _{3T3_A01}

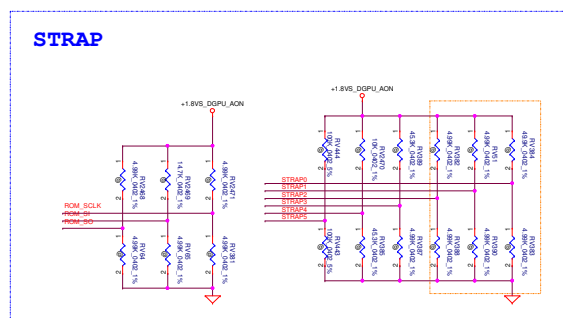













Table 6. N175-G0/G2/G3/G4 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/I _Q	Vendor	Manufacturer Part Number	Die Revision	Strip	Memory Speed Class	Date Code Alert	Qual Plan	Status
8 Gb	256M32 512M16	1.35V	Micron	MT51J2280D2P-80-B	B-die	0x9	8 Gbps	N/A	Full	Production ready
			Hynix	HY512C4UJ8-82C	A-die	0x8	8 Gbps	N/A	Full	Production ready
			Samsung	K4G80329C-HC25	C-die	0x3	8 Gbps	N/A	Full	Post-production

Notes:







- For H175-G0/G2/G3/G4, the maximum allowable memory case temperature is 85 °C.
- H175-G0/G2 memory and G0 without intent to use 5.5 Gbit/s at a later stage can also use the memory configurations in Table 4 for H175-G1.

RAM_CFG	STRAP2	STRAP1	STRAP0
0x9 (LML) M2G	 RV588 100K, 0402.5% N17_M0G0	 RV51 100K, 0402.5% N17_M0G0  RV530 100K, 0402.5% N17_M0G0	 RV935 100K, 0402.5% N17_M0G0
0xA (LMI) H2G	 RV588 100K, 0402.5% N17_M0G0	 RV51 100K, 0402.5% N17_H0G0  RV530 100K, 0402.5% N17_H0G0	 RV584 100K, 0402.5% N17_H0G0
0x3 (LH3) S2G	 RV588 100K, 0402.5% N17_S0G0	 RV51 100K, 0402.5% N17_S0G0	 RV584 100K, 0402.5% N17_S0G0

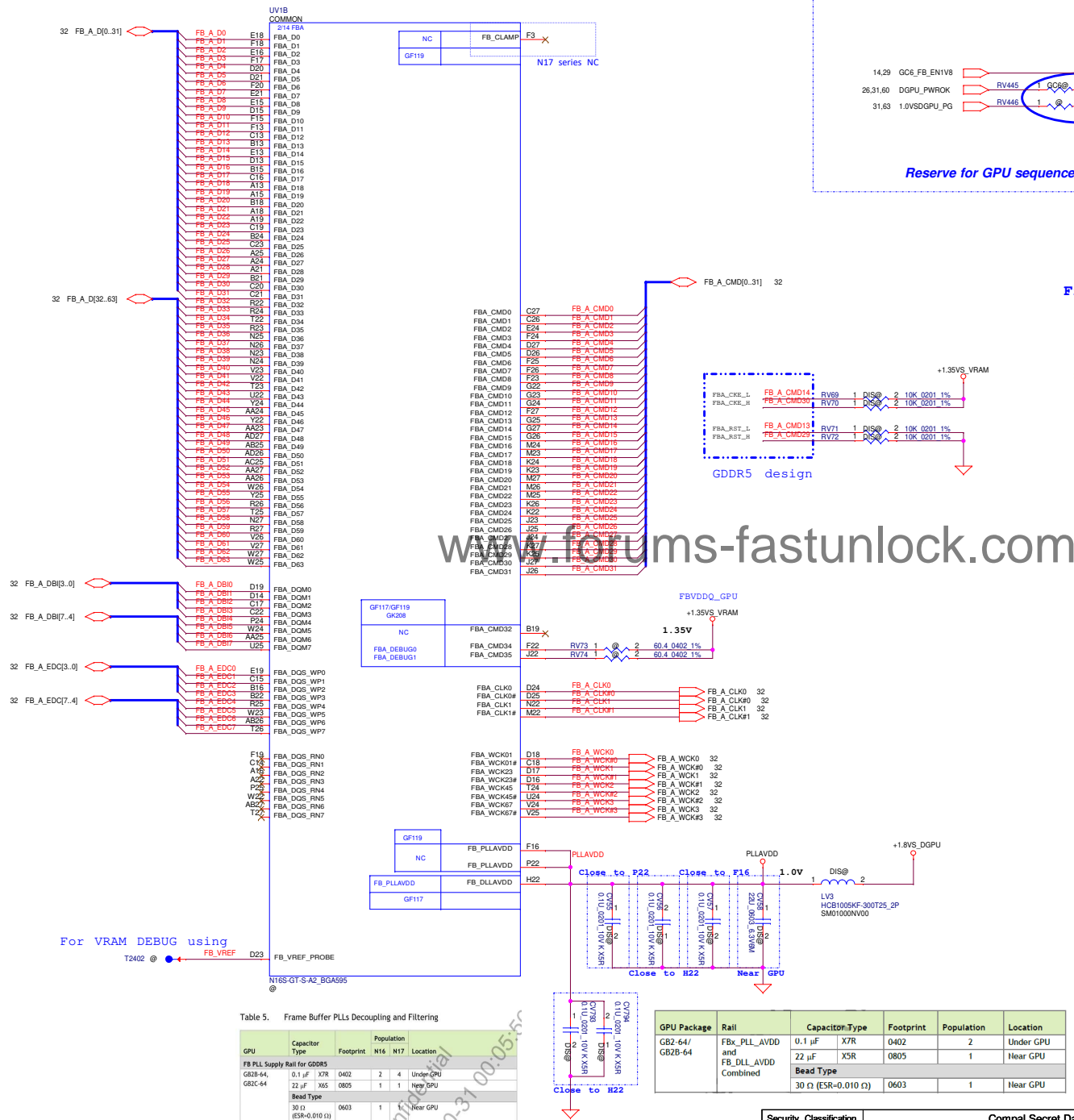
Strap Pins Note			RAMEC6 Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory config corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	H	M	9 (0x0009)
L	M	M	10 (0x000A)

Setup Pins		Resulting SDR1_EXPOSED Enable/Disable					
Row Index	ROM_S0	ROM_S1	ROM_SCLK	SDR1_EXPOSED	SDR2_EXPOSED	SDR1_EXPOSED	SDR2_EXPOSED
15	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
14	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
13	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
12	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
11	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
10	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
9	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
8	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
7	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
6	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
5	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
4	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
3	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
2	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
1	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
0	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED
15	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
14	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
13	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
12	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
11	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
10	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
9	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
8	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
7	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
6	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
5	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
4	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
3	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
2	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
1	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
0	H	H	H	DISABLED	DISABLED	DISABLED	DISABLED
All other SDR Configurations				(Reserved)			

Strap Pins			Functions Selected by this Strapping			
STRAP3	STRAP4	STRAP3	SWB_ALT_ADDN	DEVID_SEL	PCIE_CFG	YGA_DEVICE
L	L	L	0	0	0	0
L	L	H	0	0	0	1
L	H	L	0	0	1	0
L	H	H	0	0	1	1
H	L	L	0	1	0	0
H	L	H	0	1	0	1
H	H	L	0	1	1	0
H	H	H	0	1	1	1

ROM_SO	ROM_SI	ROM_SCLK	STRAP5	STRAP4	STRAP3
 RV2468 DiSP 100K_0402_5%	 RV2469 DiSP 100K_0402_5%	 RV2471 DiSP 100K_0402_5%	 RV443 DiSP 100K_0402_5%	 RV385 DiSP 100K_0402_5%	 RV287 DiSP 100K_0402_5%

Note: The ternary strap pins listed in the Strap Pins columns must be pulled to one of three voltage levels. "L" means Low level (GND). "M" means middle level (0.9V). "H" means High level (1.8V).



The three diagrams illustrate different ways to connect the 1.0V5 DQPU pin to the 1.0V5 DQPU_EN pin:

- Diagram 1 (Left):** Shows a direct connection between the 1.0V5 DQPU pin and the 1.0V5 DQPU_EN pin. The 1.0V5 DQPU pin is connected to the 1.0V5 DQPU_EN pin through a 10k resistor.
- Diagram 2 (Middle):** Shows a connection between the 1.0V5 DQPU pin and the 1.0V5 DQPU_EN pin through a 10k resistor. The 1.0V5 DQPU pin is connected to the 1.0V5 DQPU_EN pin through a 10k resistor.
- Diagram 3 (Right):** Shows a connection between the 1.0V5 DQPU pin and the 1.0V5 DQPU_EN pin through a 10k resistor. The 1.0V5 DQPU pin is connected to the 1.0V5 DQPU_EN pin through a 10k resistor.

Reserve for GPU sequence tuning

Products	VRAM Type	GPU Core	GPU FBIO		FB Total ^{1, 2}		1.05V Total ³	3.3V Total
		—	1.5V ⁴	1.35V ⁴	1.5V ⁴	1.35V ⁴	1.05V ⁴	3.3V ⁴
		(A)	(A)	(A)	(A)	(A)	(A)	(A)
N165-GMR	GDDR5	19.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	21.0	1.4	1.4	2.4	2.3	0.80	0.06
N165-GTR	GDDR5	26.0	—	2.0	—	4.2	0.80	0.06
	DDR3/L	26.0	1.4	1.4	2.4	2.3	0.80	0.06

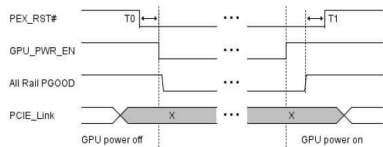
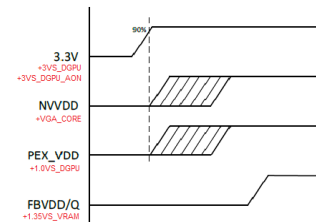


Table 18-1. Optimus Timing Parameters

Symbol	Description	Min	Max	Units
T0	PEX_RST# assertion to GPU_PWR_EN=0	>0	5	ms
T1	All GPU power rail up and stable to PEX_RST# de-assertion	0.1	5	ms

GPU	Capacitor Type	Footprint	Population		Location
			N16	N17	
N16 X33_MAM (N17 Y0D0N18) Supply Rail					
GR2B-64,	0.1 μF X7R	0402	2	2	Under GPU
GR2C-64	1.0 μF X6S	0603	1	1	Near GPU
	4.7 μF X6S	0603	1	1	Near GPU
N16 X33_AON (N17 V18_AON) Supply Rail					
GR2B-64,	0.1 μF X7R	0402	1	2	Under GPU
GR2C-64	1.0 μF X6S	0603	1	1	Near GPU
	4.7 μF X6S	0603	1	1	Near GPU



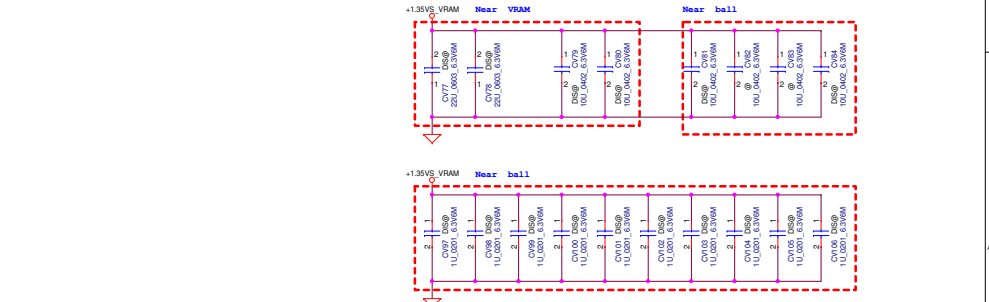
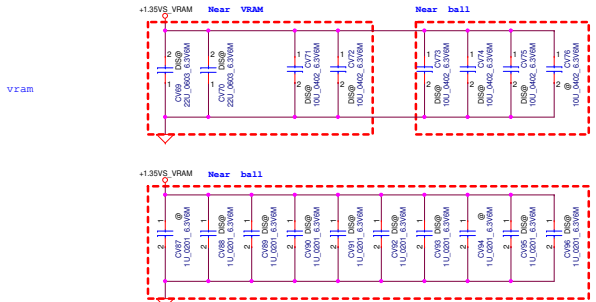
- 3.3V includes all rails powered at 3.3V; PEX_VDD includes all rails that are shared on 1.05V/1.0V
- The ramp time for any rail must be more than 40 μ s and is recommended to be less than 2 ms.

Timing diagram for the PEX to GDS interface. The diagram shows the relationship between various signals during GDS Entry and GDS Exit phases. FB_CKE transitions from Normal to Self-Refresh and back. PEX_LINK transitions from Active to X and back. GPU_PEX_RST# is active low. GDS_FB_EN is active low. VV3_MAIN_EN is active low. All Rail PGOOD is active low. GPU_EVENT# is active low. The GDS Entry phase is marked by a vertical dashed line, and the GDS Exit phase is marked by another vertical dashed line. A 'Detect' event is shown on the PEX_LINK signal during the Self-Refresh phase, with a 'Tdet' delay indicated. A 'T0' delay is indicated for the GPU_EVENT# signal during the GDS Exit phase.

Symbol	Description	Min	Max	Unit
T0	GPU_EVENT# assertion period	0.001	N/A	ms
T1	3V3_MAIN_EN assertion to all power rails up and stable	0.04	4	ms

- All RAIL PG00=1 represents all GPU power rails are ramped up and in regulation. If any GPU power rail cannot be guaranteed in regulation this state should equal to 0.
- During GPU exit, the order of power rail ramp-up must follow the power-up sequence described in Chapter 3 with the exception that FBVDD/Q stays on.
- All delays should be minimized to increase time spent in G6s for maximum power saving.
- The entire entry/exit sequence must complete within 200 ms.

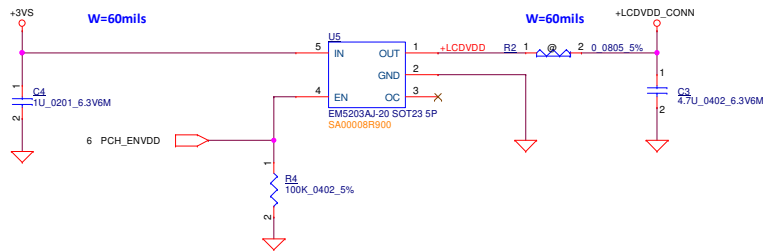
Table 7-4. GDDR5 Mode H Mapping



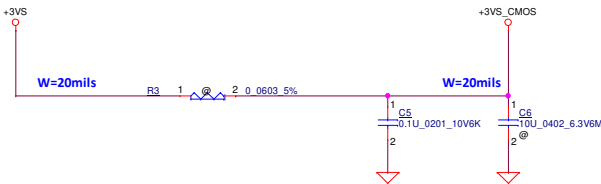
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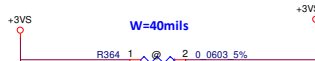
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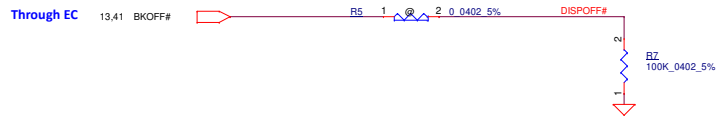
CAMERA POWER CIRCUIT



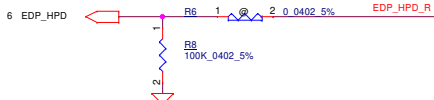
IR POWER



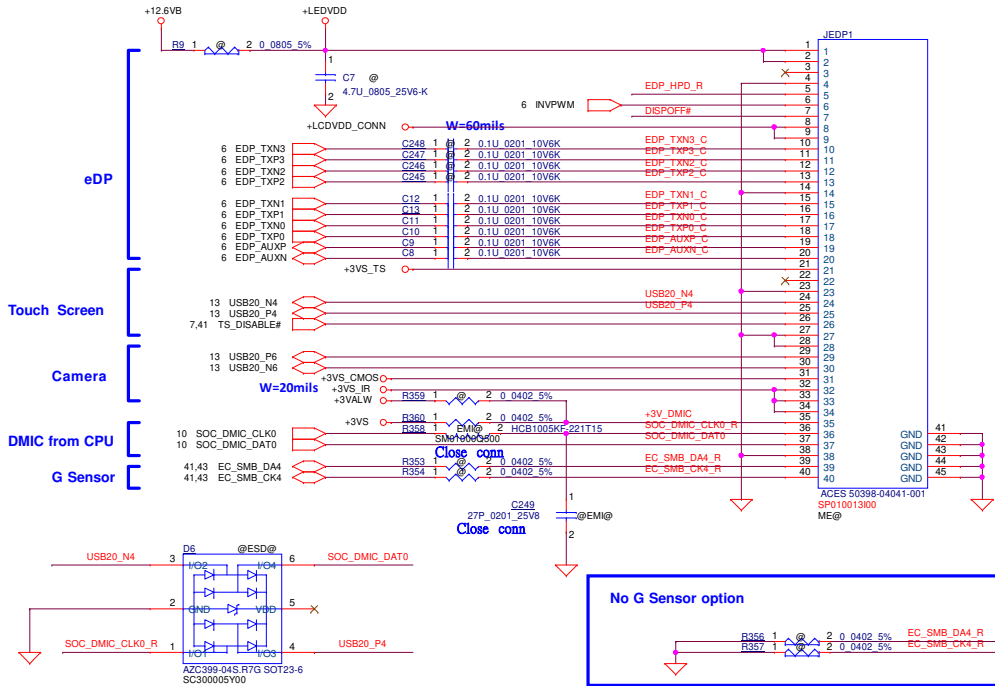
DISPLAY OFF



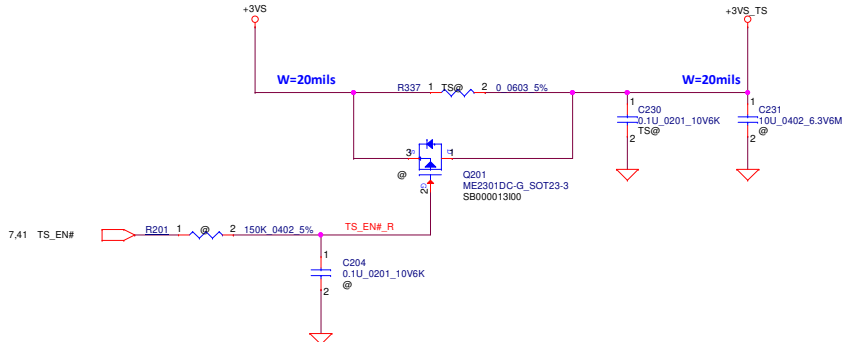
HOT PLUG DETECT



eDP CONNECTOR



Touch Screen POWER CIRCUIT

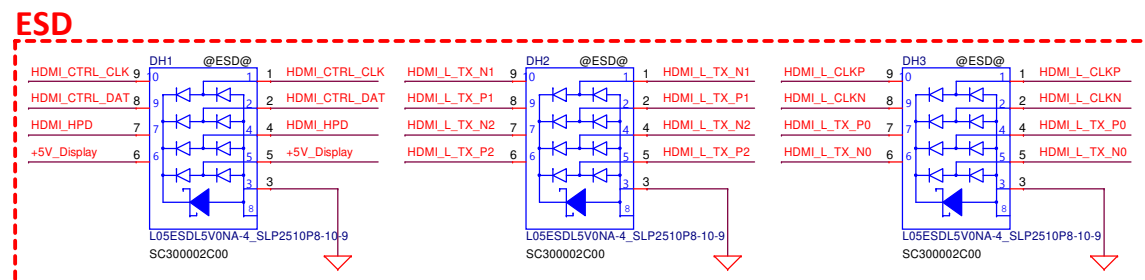
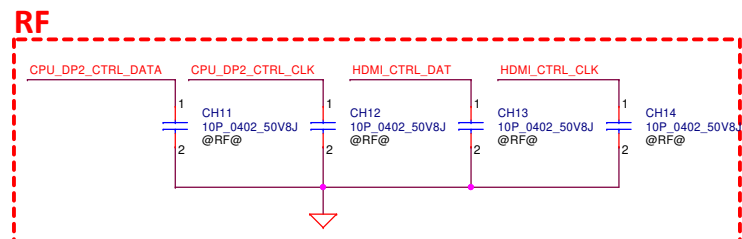
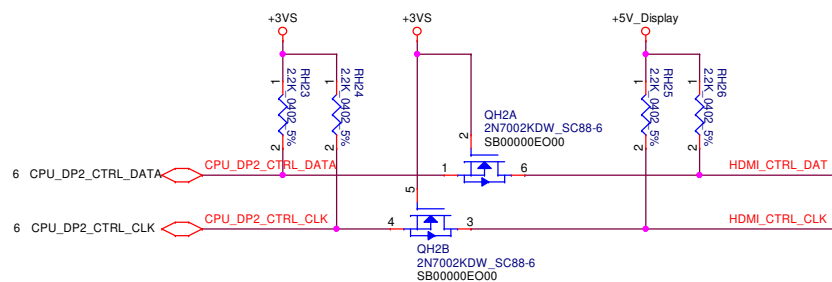
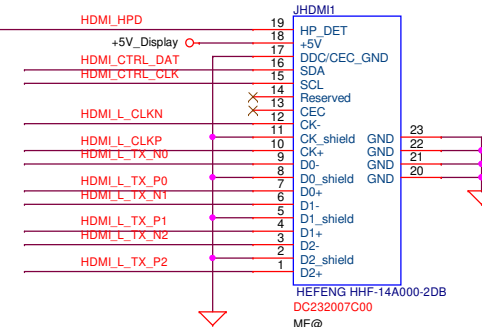
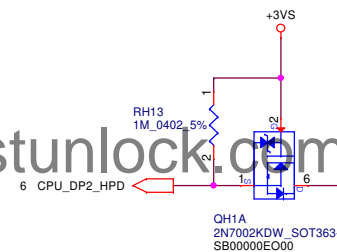
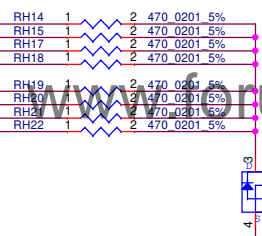
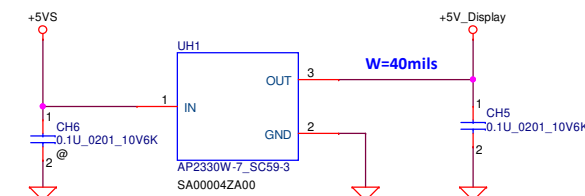
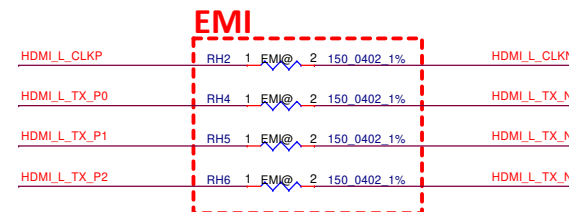
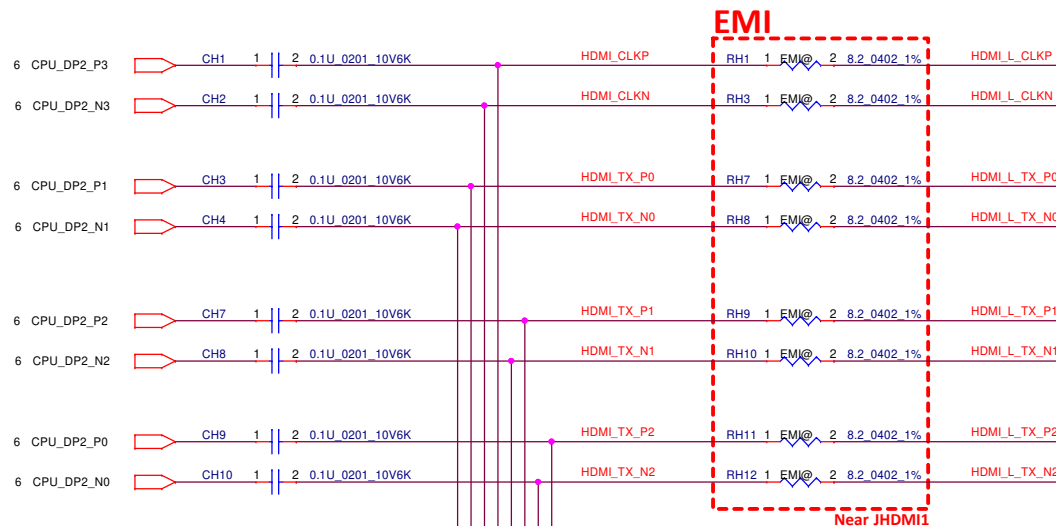


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HDMI



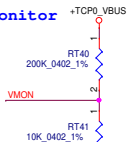
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Slave Addresss setting

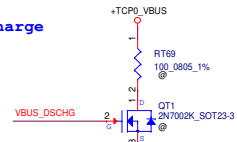
Slave Addr	Na	Nb	Nc	Nd
addr0:0x00	00	00	00	00
addr1:0x01	01	01	01	01
addr2:0x02	02	02	02	02
addr3:0x03	03	03	03	03

It's used for SMBUS slave addr0/1/2/3 setting during power on initialization.

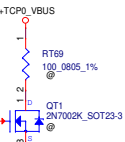
VBUS Voltage/current Monitor



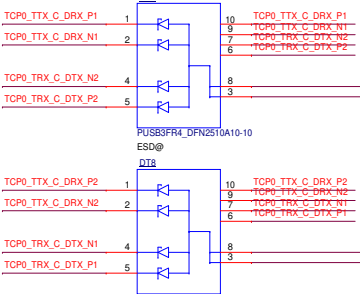
VBUS Discharge



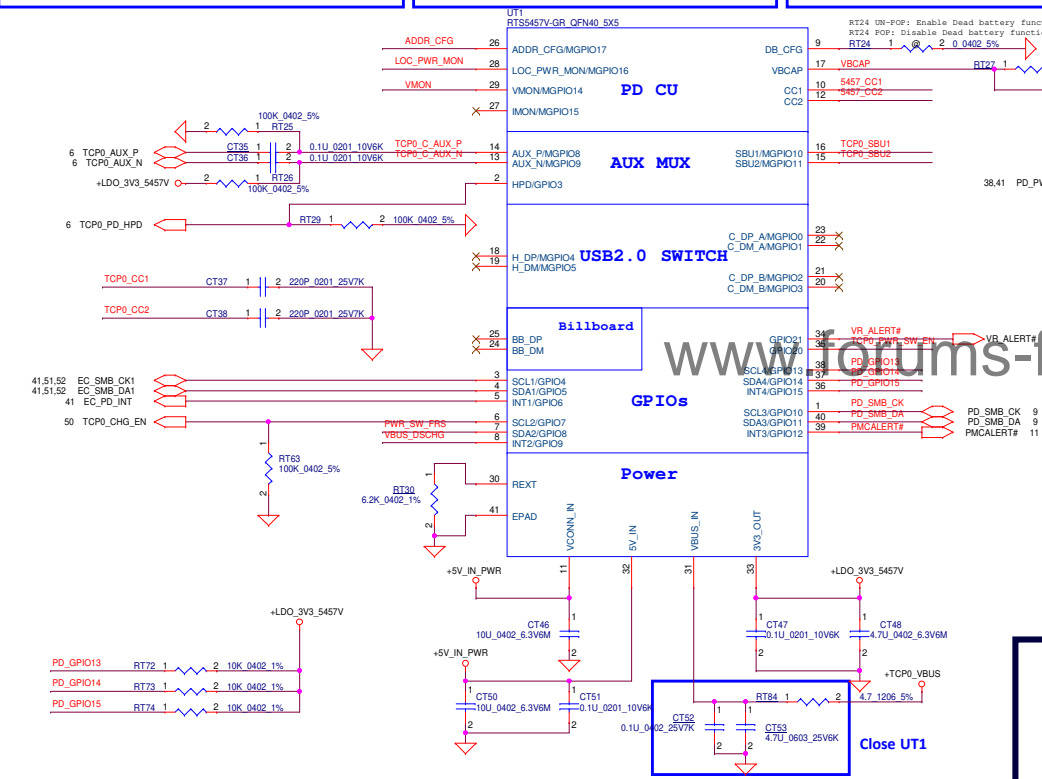
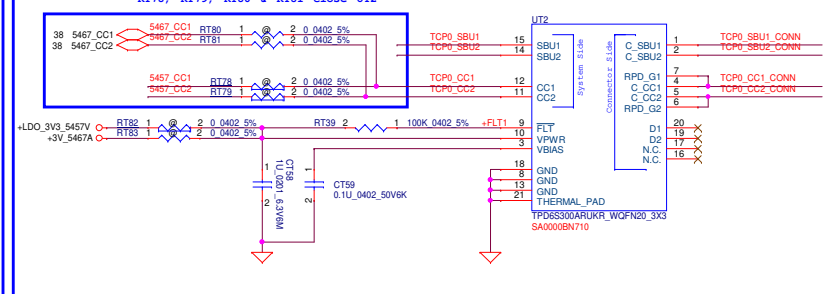
Local PWR Voltage Monitor



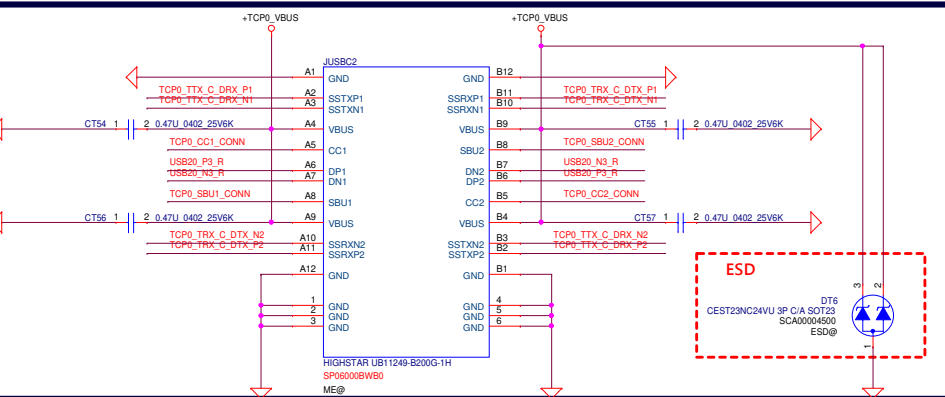
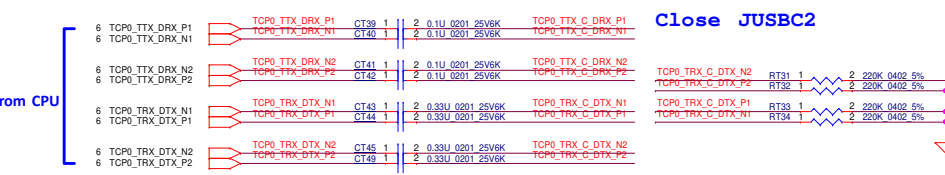
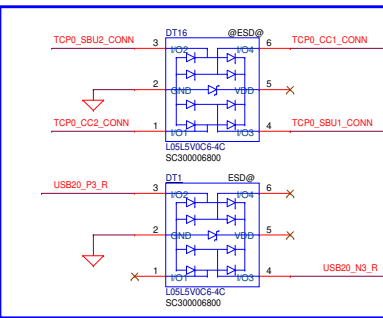
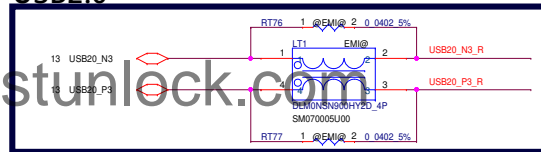
Close JUSBC2



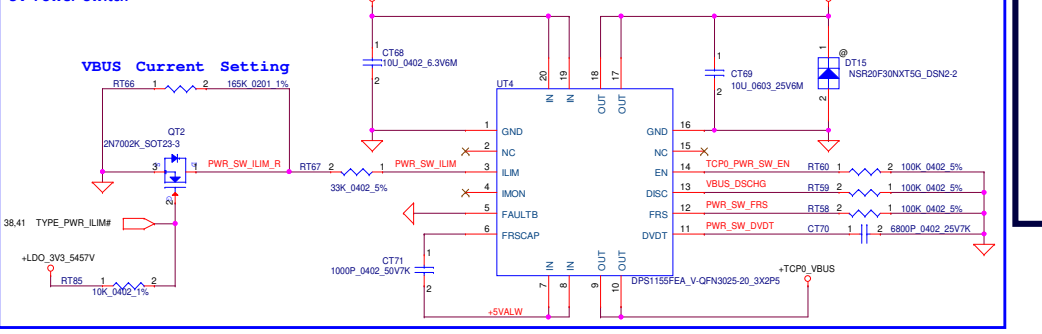
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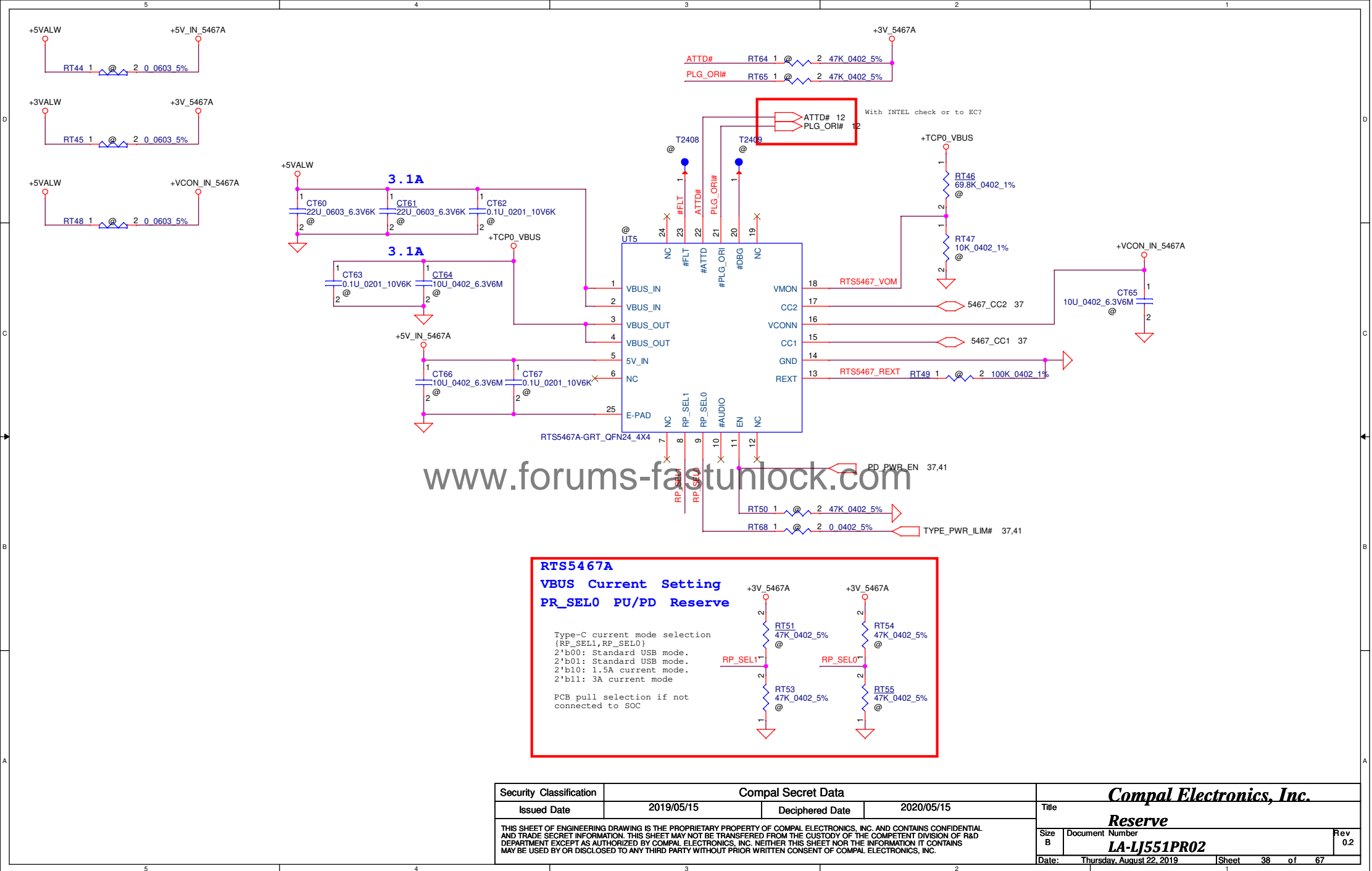


USB2.0



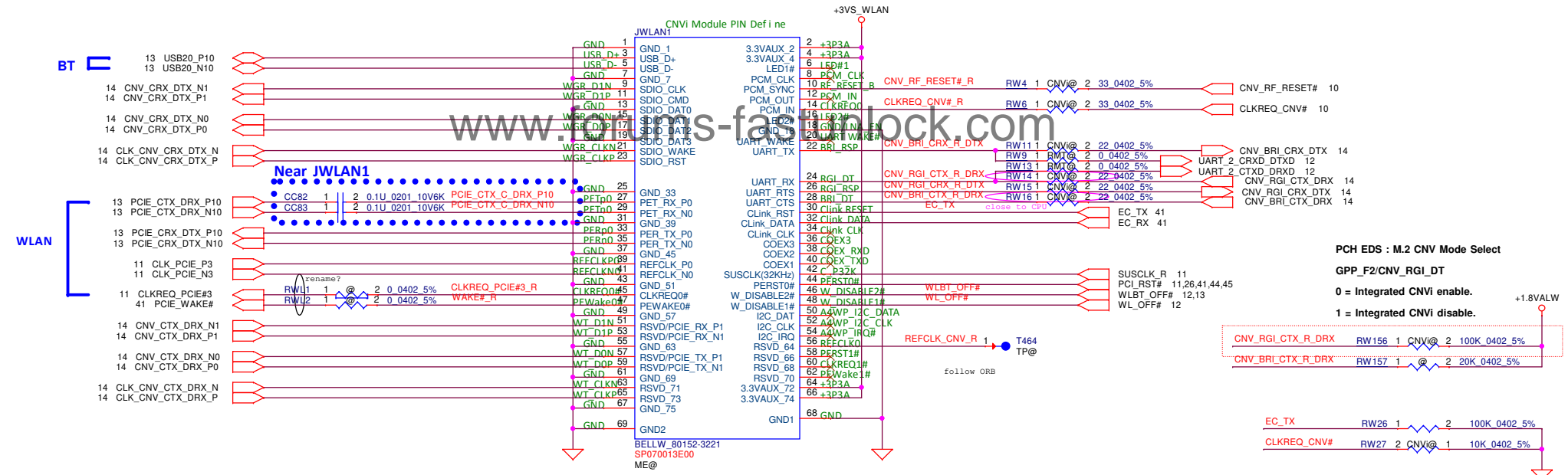
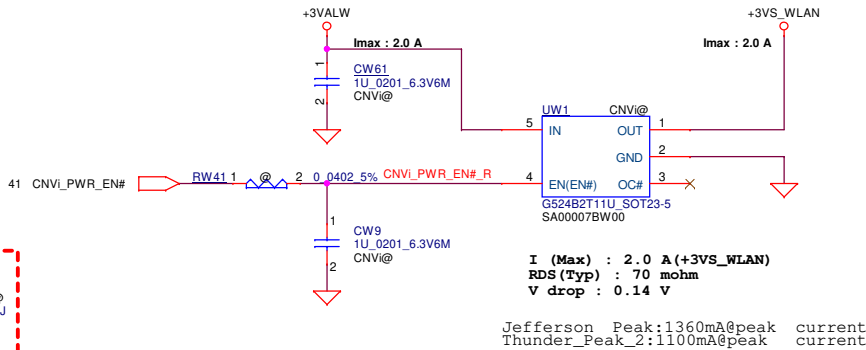
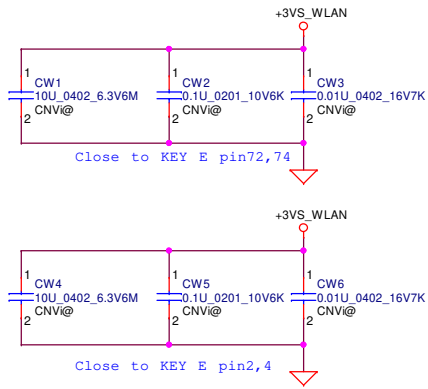
5V Power Switch



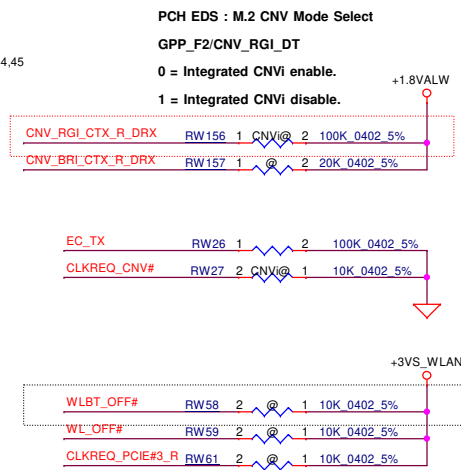


NGFF WLAN / BT (Key E)

NGFF Wireless LAN / BT (Key E) [PCIE+USB/CNVi]

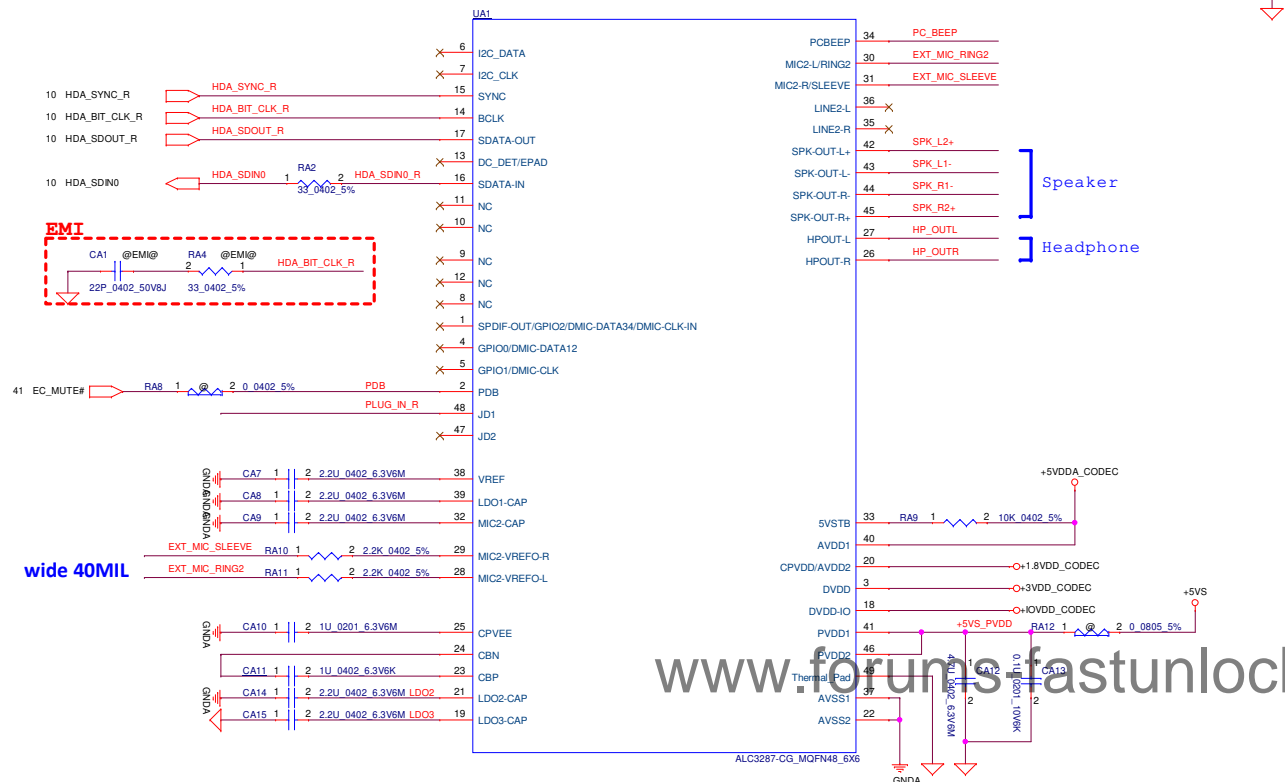


Note: The real behavior of BT_DISABLE are
BT_DISABLE=LOW, BT=OFF
BT_DISABLE=HIGH, BT=ON

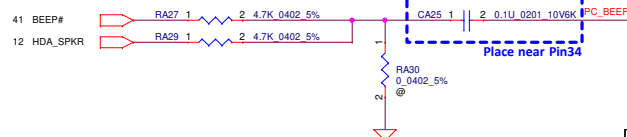
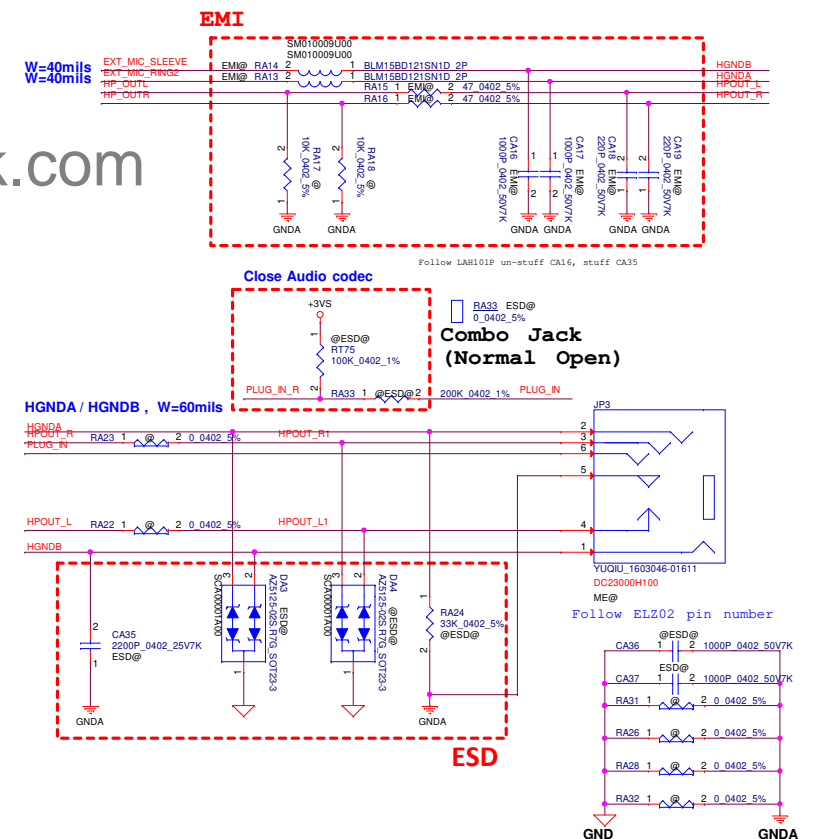
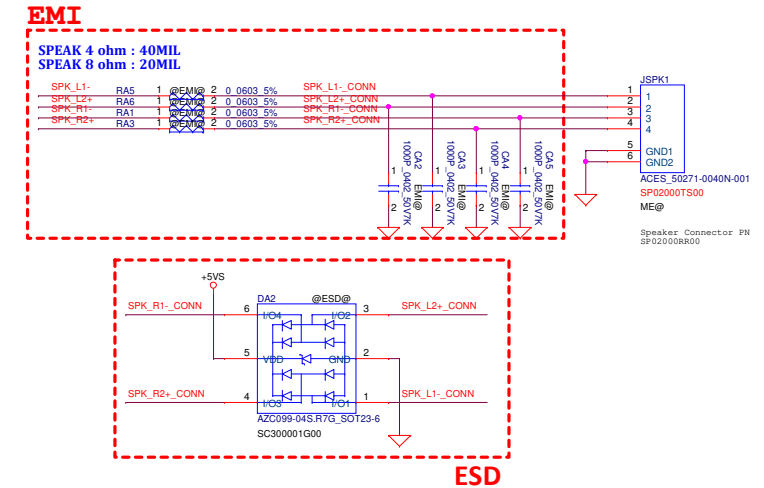


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						Size		Document Number		Rev	
						LA-LJ551PR02		0.2			
Date:		Thursday, August 22, 2019		Sheet		39		of 67			

ALC3287

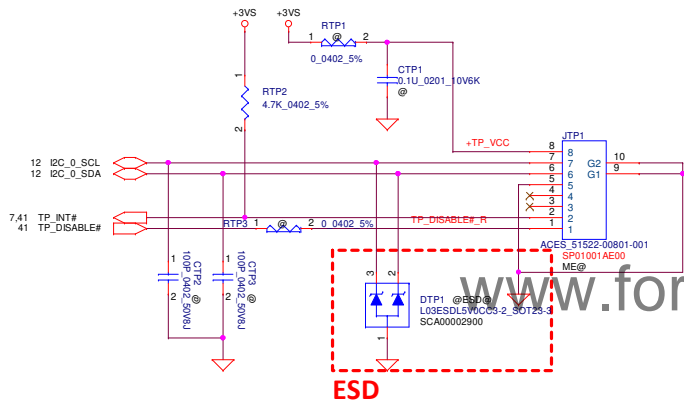


Speaker

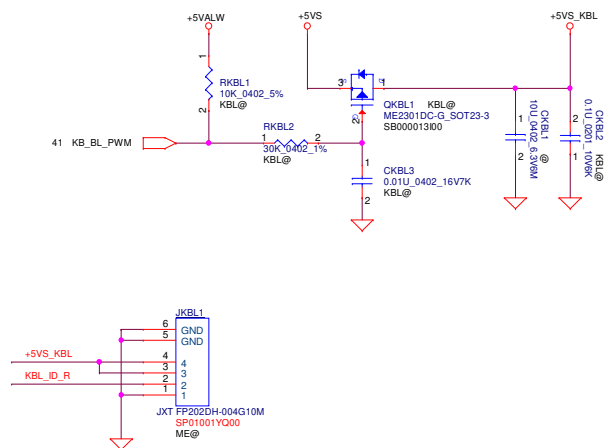


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				LA-IJ551PR02	
				Date:	Thursday, August 22, 2019
				Sheet	40 of 67

Touch Pad

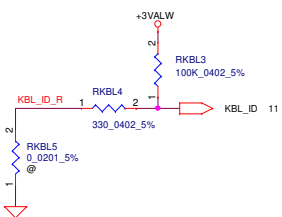


Keyboard Backlight

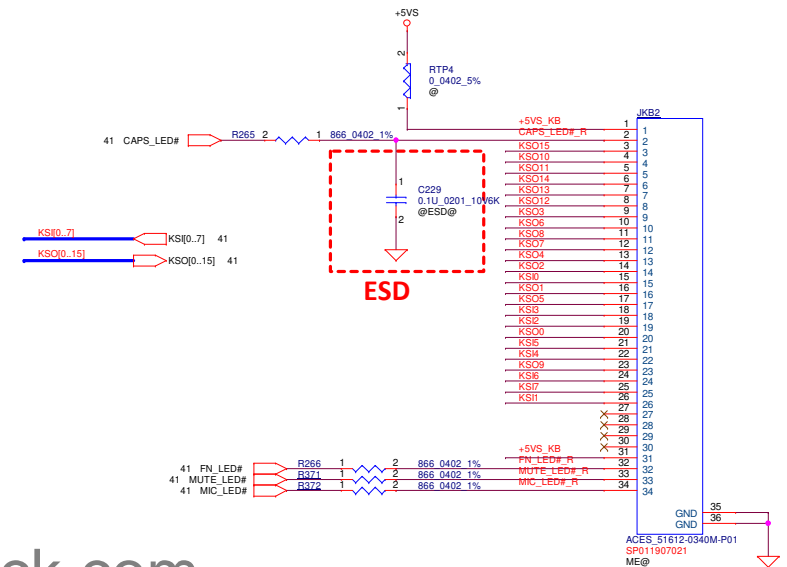


Keyboard BackLight_SELECT

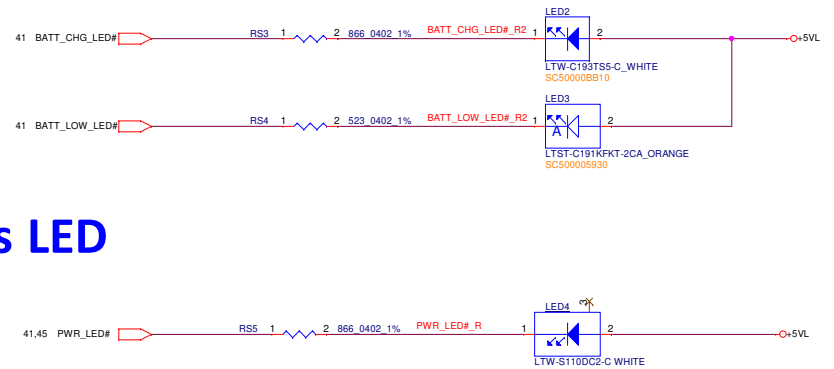
Function	KBL_ID
KBL	0
NO KBL	1



Keyboard



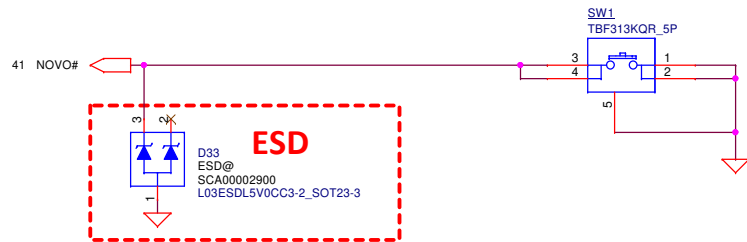
BATT LED



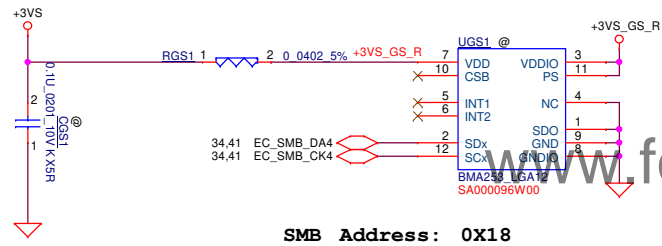
Status LED

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						KB / LED / TP / LID				
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NOVO Button

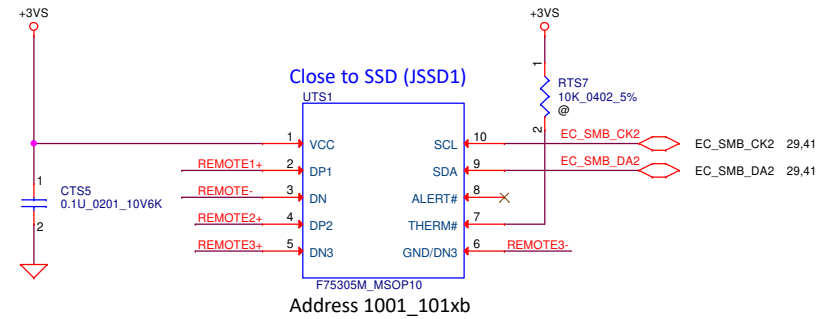


G-Sensor

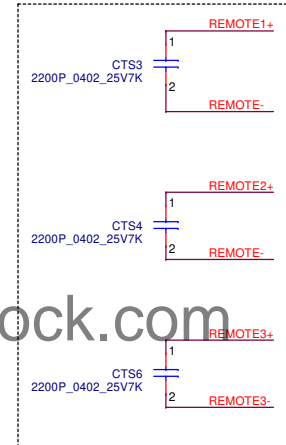


SMB Address: 0X18

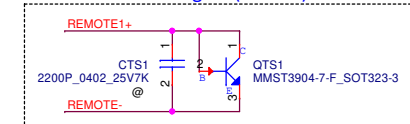
Thermal Sensor



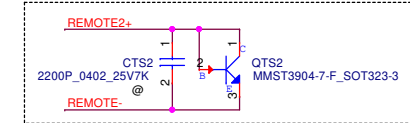
Close to UTS1



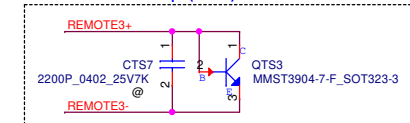
Close to BATT Charger (JBATT1)



Close to WLAN (JWLAN1)



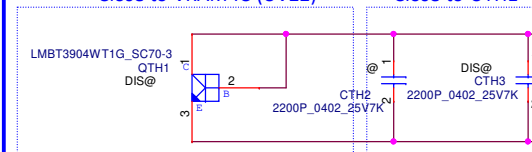
Close to CPU Chip (UC1)



REMOTE1,2,3 (+/-) :
Trace width/space:10/10 mil
Trace length:<8"

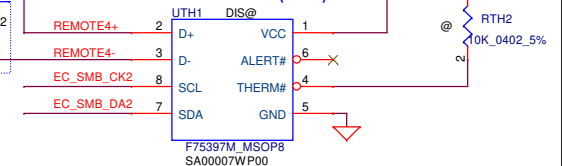
Close to VRAM IC (UV22)

Close to UTH1



REMOTE4(+/-) :
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Trace length:<8"

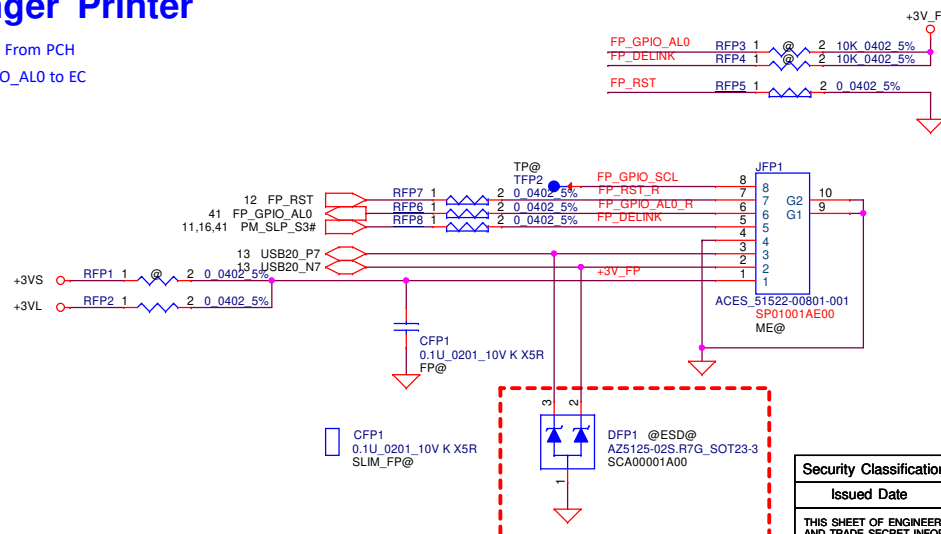
Close to GPU (UV1)



Address 1001_100xb

Finger Printer

FP_RST From PCH
FP_GPIO_AL0 to EC



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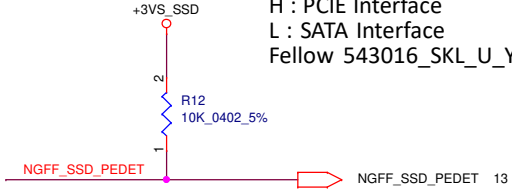
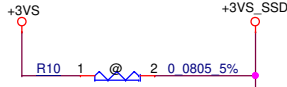
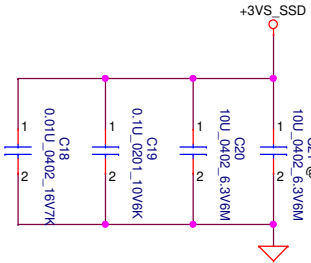
SSD (TYPE M)

SSD PCIE

SSD SATA

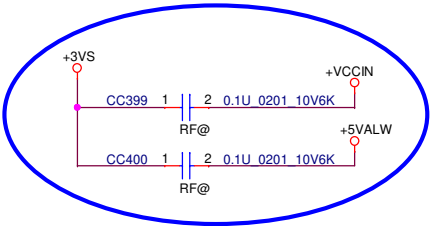
- 13 PCIE_CRX_DTX_N13
- 13 PCIE_CRX_DTX_P13
- 13 PCIE_CTX_DRX_N13
- 13 PCIE_CTX_DRX_P13
- 13 PCIE_CRX_DTX_N14
- 13 PCIE_CRX_DTX_P14
- 13 PCIE_CTX_DRX_N14
- 13 PCIE_CTX_DRX_P14
- 13 PCIE_CRX_DTX_N15
- 13 PCIE_CRX_DTX_P15
- 13 PCIE_CTX_DRX_N15
- 13 PCIE_CTX_DRX_P15
- 13 PCIE_CRX_DTX_N16
- 13 PCIE_CRX_DTX_P16
- 13 PCIE_CTX_DRX_N16
- 13 PCIE_CTX_DRX_P16

- 11 CLK_PCIE_N1
- 11 CLK_PCIE_P1



NGFF_SSD_PEDET#
H : PCIe Interface
L : SATA Interface
Fellow 543016_SKL_U_Y_PDG_0_9

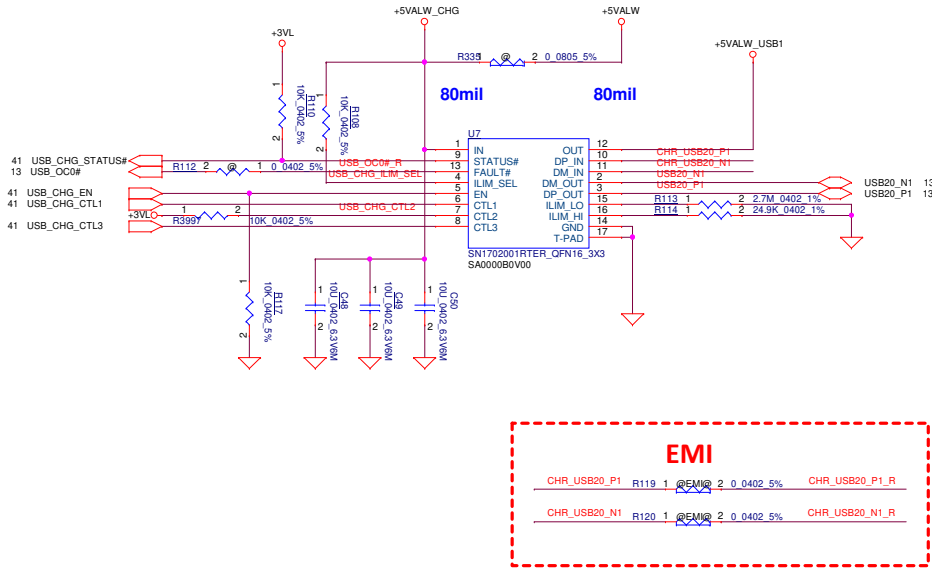
For RF team cross mote



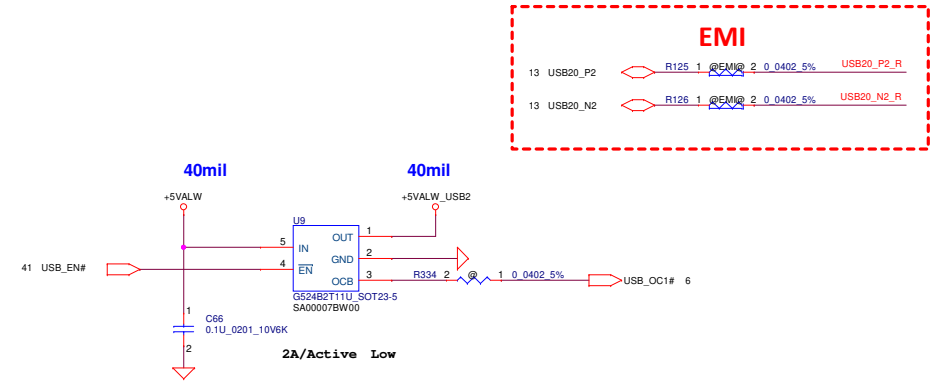
www.forums.netunlock.com

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				LA-LJ551PR02				0.2
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USB3.0_Port (AOU_Port)



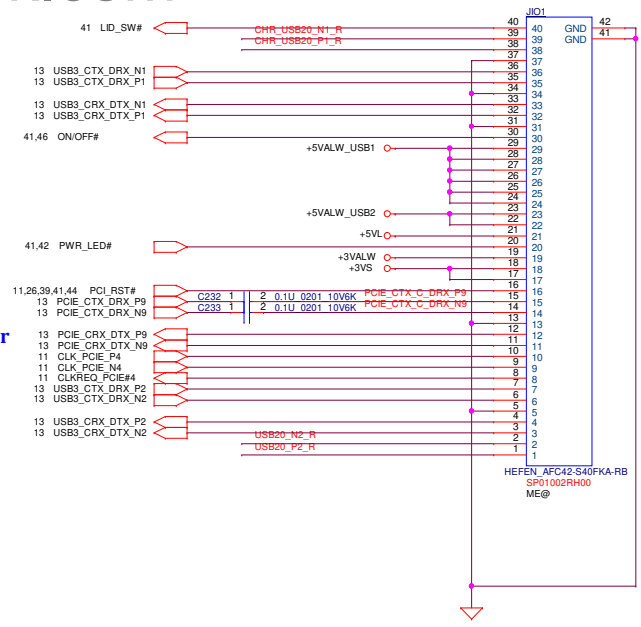
USB3.0_Port (Non-AOU_Port)



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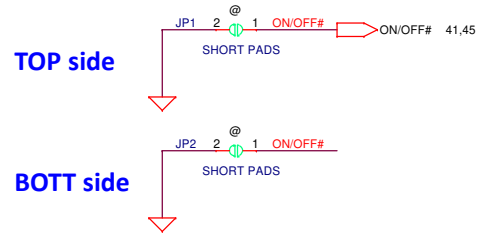
I/O CONN

Card Reader

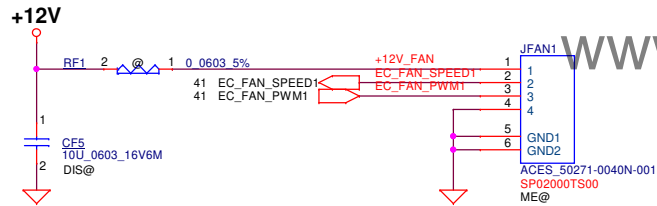


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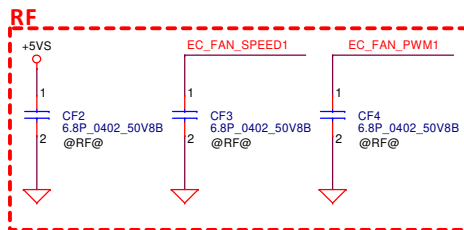
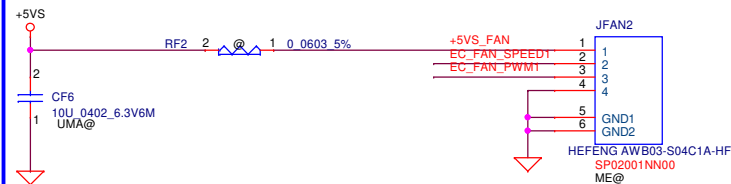
ON/OFF# SHORT PAD



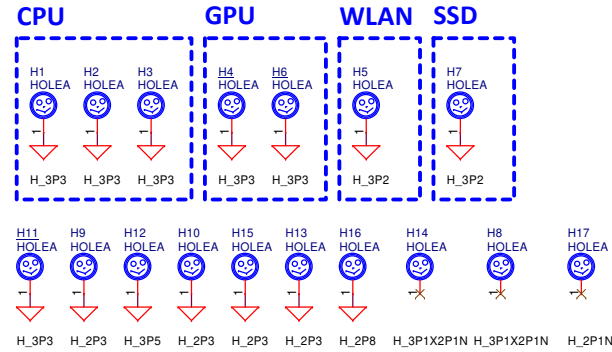
+12V FAN



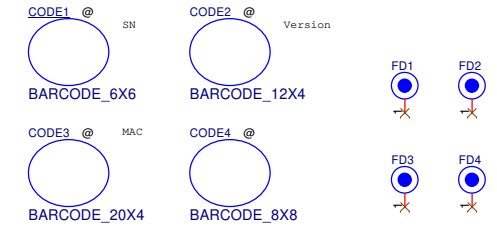
+5V FAN



SCREW

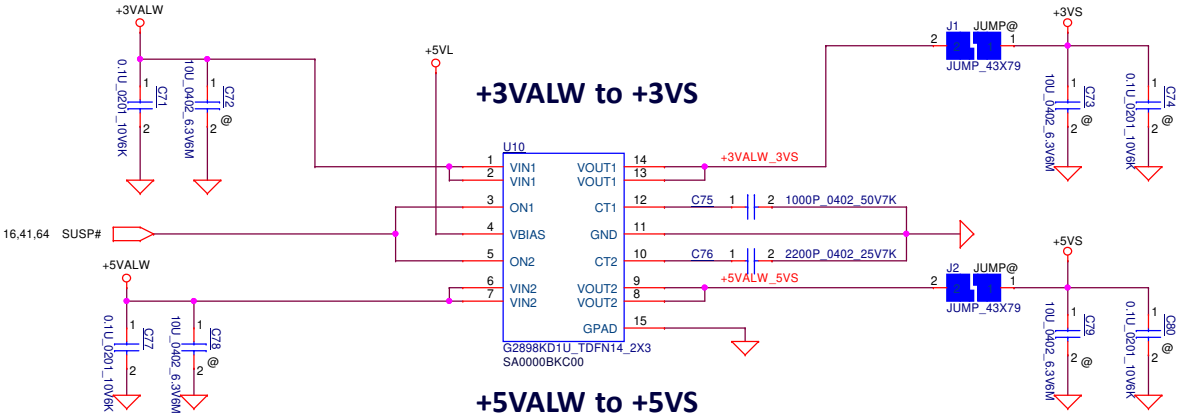


LASER BARCODE



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DC to DC



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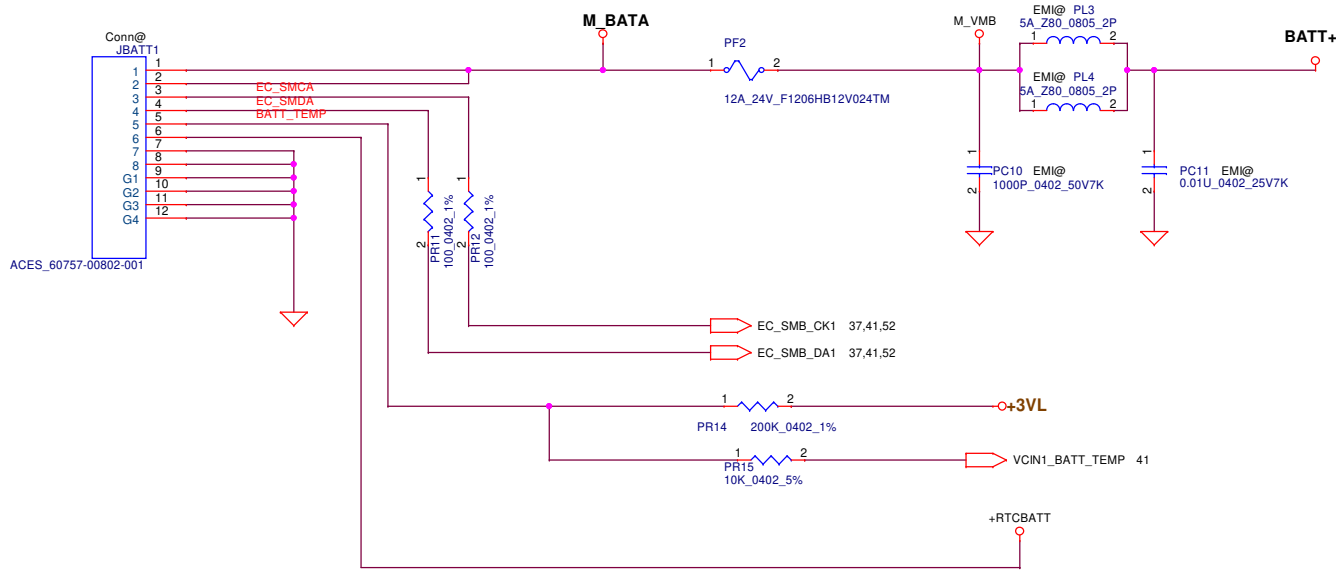
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				Document Number	0.2
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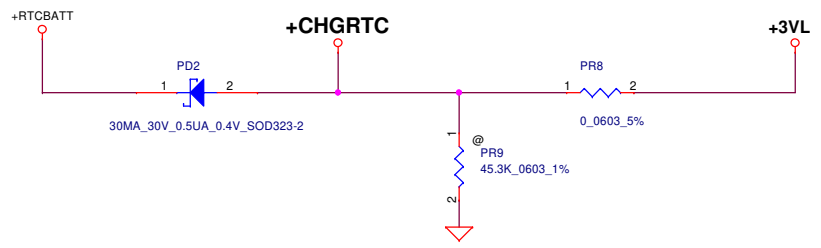
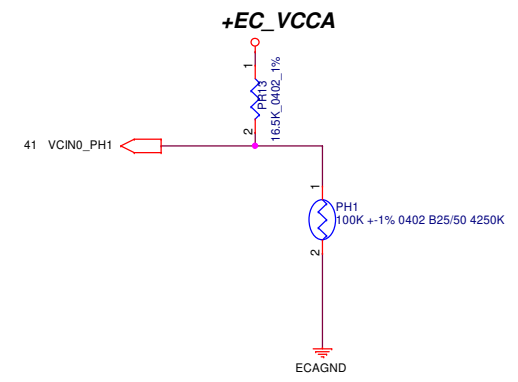
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				Size B	Document Number	Rev 0.2
				Date:	Thursday, August 22, 2019	Sheet 49 of 67

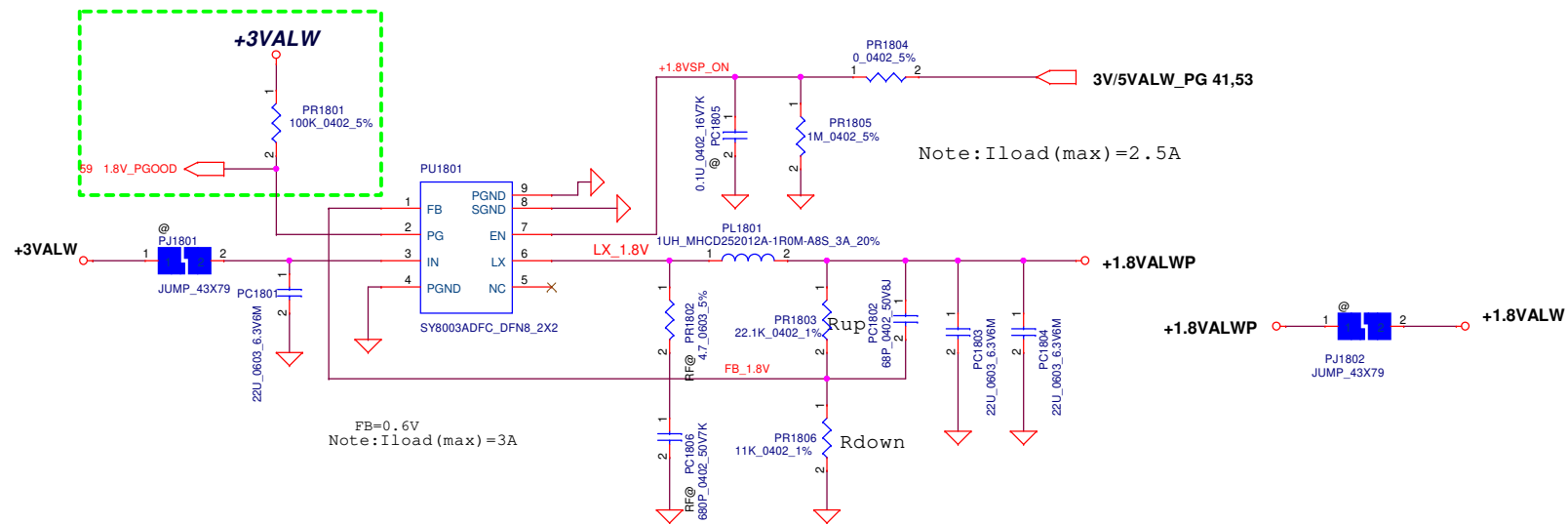


PH201 under CPU botten side :
CPU thermal protection at 93 +-3 degree C
Recovery at 56 +-3 degree C



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Note:
When design Vin=5V, please stuff snubber
to prevent Vin damage

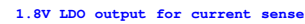
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MP2940_V1A.mdd for IC portion
MP2940_V1B.mdd for SW portion

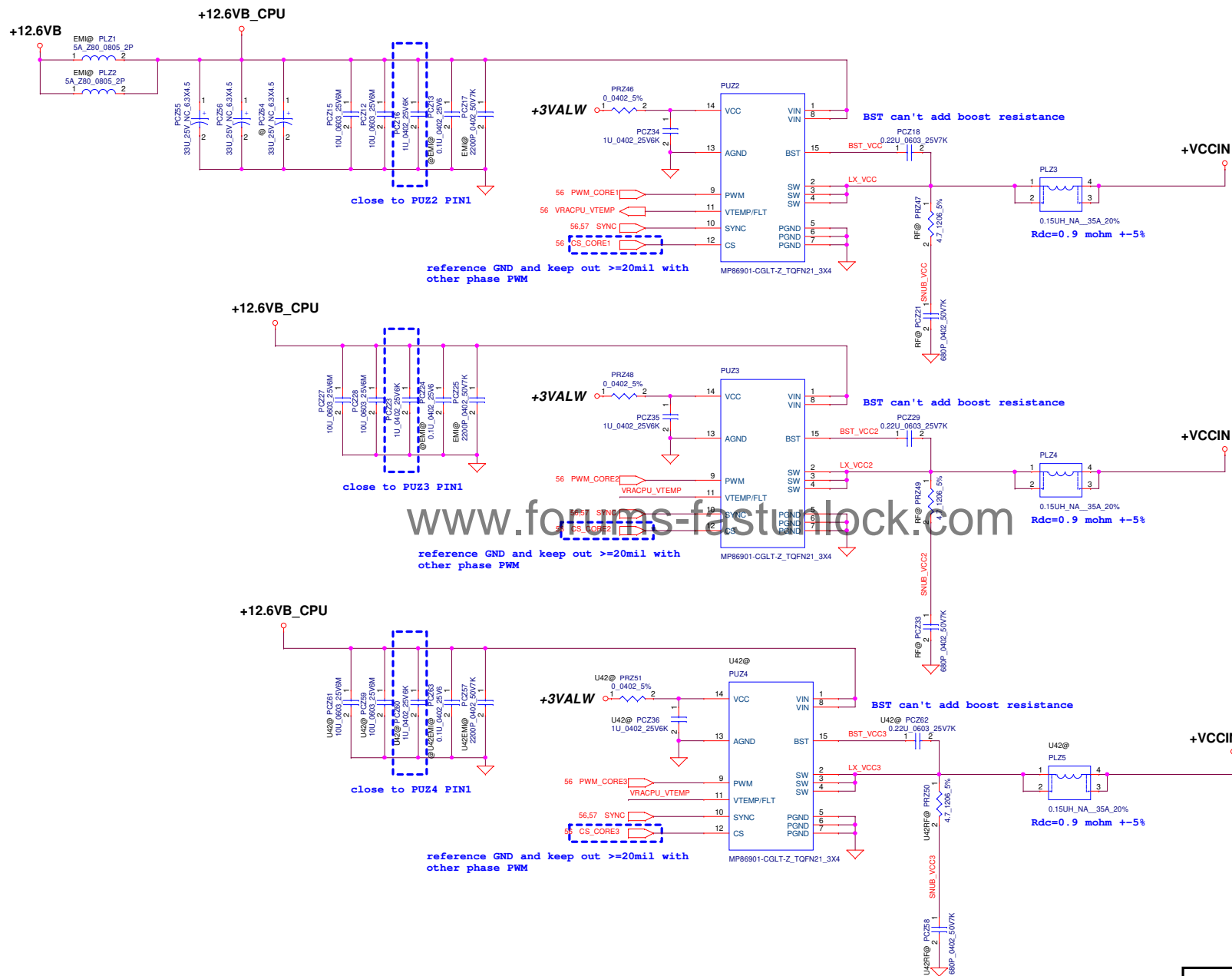
Where:
PWR_in_Max is the maximum input power, with the unit of W.

$$T_{\text{JUNCTION}} = \frac{V_{\text{TEMP}} + 100\text{mV}}{10\text{mV}/^{\circ}\text{C}}$$



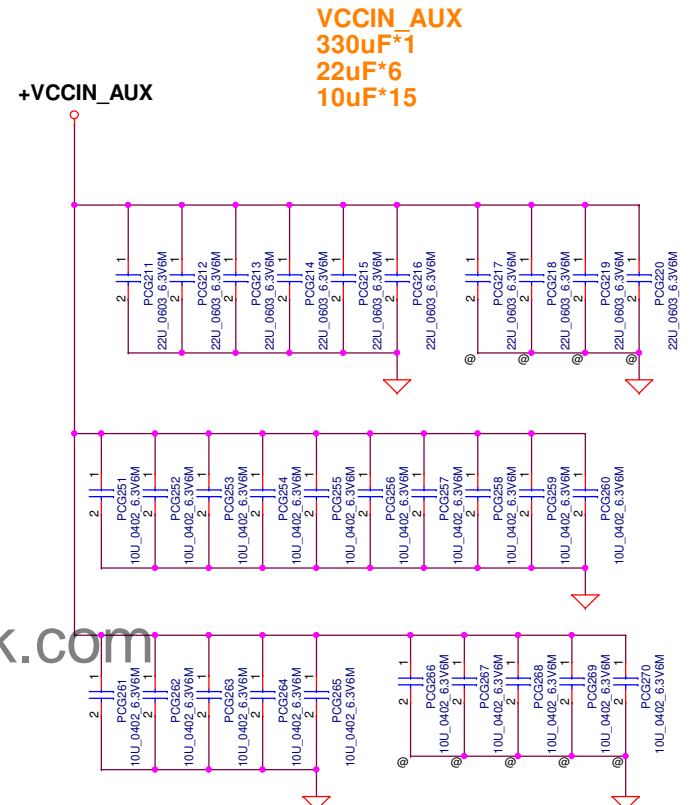
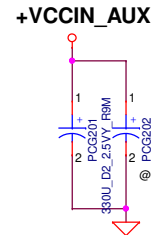
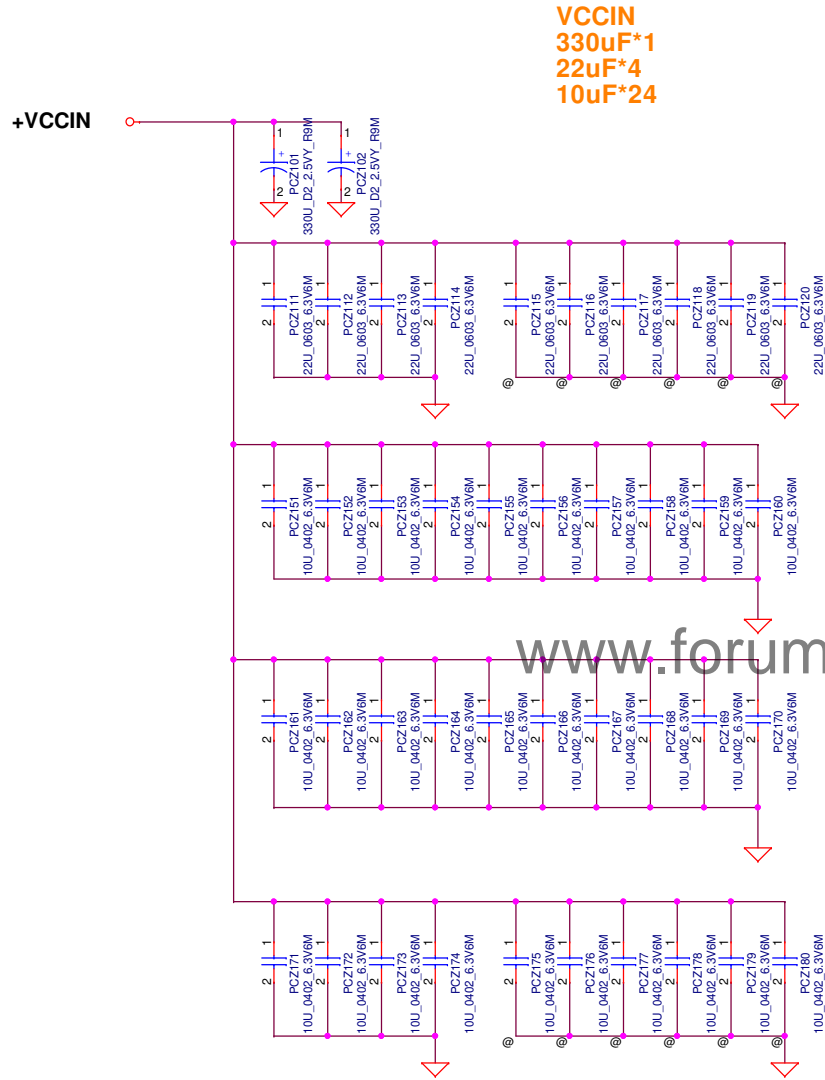
	Compal Electronics, Inc.
Title	PWR- VCORE(MP2940)

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Function Field :
 Drivers:36.2
 Rest of support elements:36.3
 CPU_Core output CAP (Including MLCC):36.4

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Issued Date	2019/05/23	Deciphered Date	2021/05/31	Size	Document Number
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Size	Document Number	Rev		Date	
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CPU PWR controller(36.1), Driver MOS(36.2), Support component(36.3)

Module model information
MP2941_V1.mdd

VCCIN_AUX (Base on PDG rev 0.71)
Peak Current 26A (ICCmax)
TDC :10A
DC Load line :TBD mV/A
AC Load line :TBD mV/A
OCP Current 32A
Fsw=700kHz

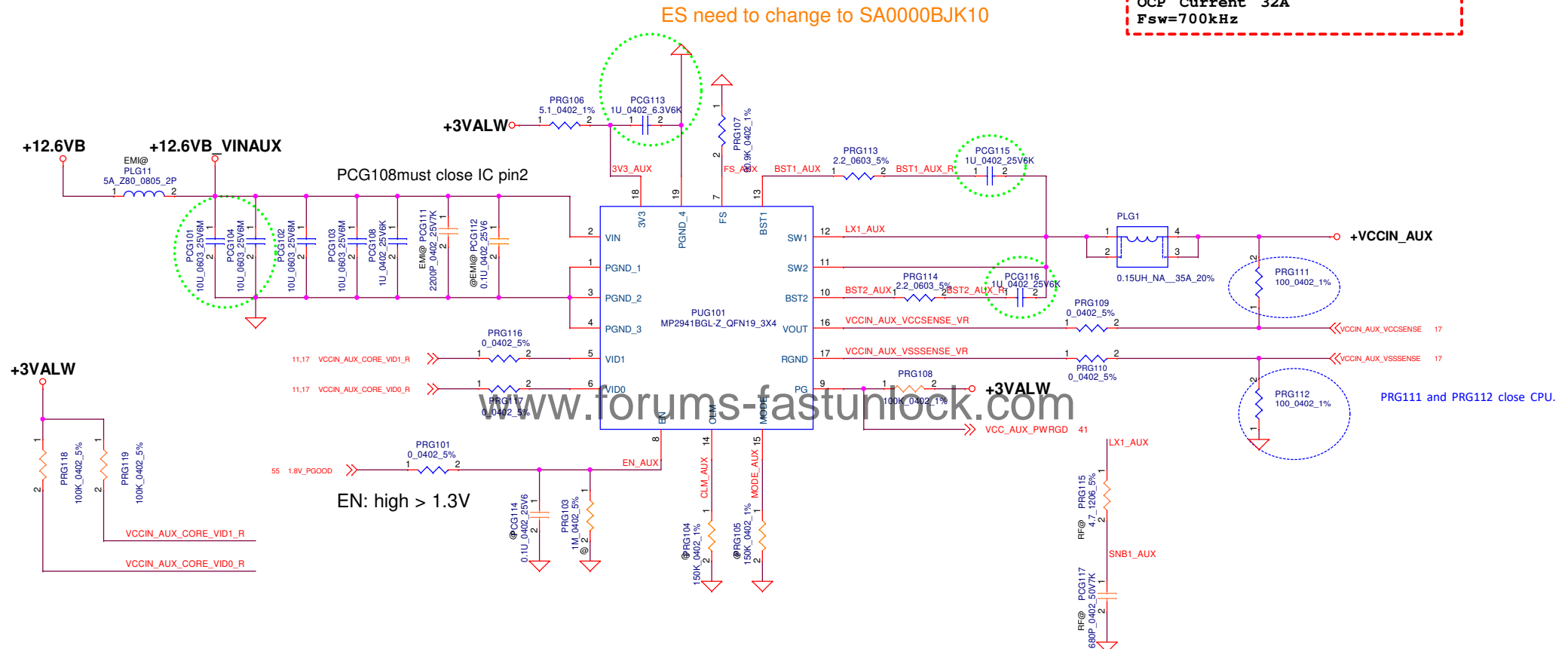


Table---1:VID control Bit logics

VID1	VID0	VOUT(V)
0	0	0
0	1	1.1
1	0	1.65
1	1	1.8

Table---2:CLM Select

State	CLM	Resistor to GND
M1	7A	0
M2	10A	90k
M3	13A	150k
M4	17A	>230k or float

Table---3:MODE Select

State	Interleaving	VID Down option	Resistor to GND
M1	N	Slew down	0
M2	Y	Slew down	90k
M3	Y	Decay	150k
M4	N	Decay	>230k or float

Table---4:FS Select

State	Fs(kHz)	Resistor to GND
M1	500	0
M2	700	90k
M3	1000	150k
M4	1200	>230k or float

TBD under checking with MPS

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R1, R2, R3, R4, R5, C are based on VGA type to set.

OpenVReg Configurations:(PSI pin)

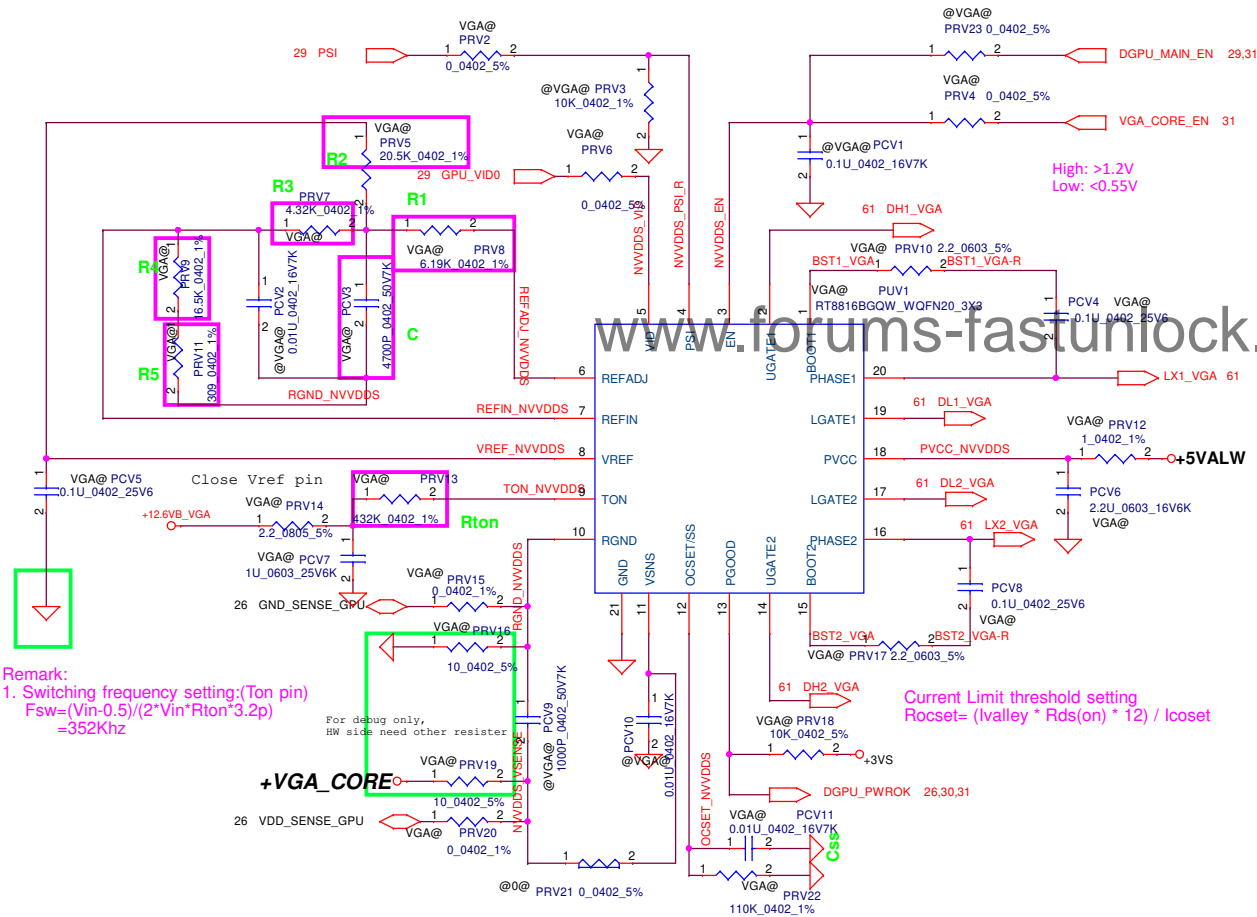
Operation phase Number	PSI Voltage setting
1 phase with DEM	0V to 0.4V
1 phase with CCM	0.7V to 0.88V
2 phase with DEM	1.08V to 1.35V
2 phase with CCM	1.6V to 5.5V

PSI pull up on HW side

$V_{boot} = V_{vref} * R_{ref2} / (R_{ref1} + R_{ref2} + R_{boot})$
 $R_t = R_{refadj} // (R_{boot} + R_{ref2})$
 $V_{min} = V_{vref} * [R_{ref2} / (R_{ref2} + R_{boot})] * [R_t / (R_{ref1} + R_t)]$
 $V_{max} = V_{vref} * R_{ref2} / [(R_{ref1} // R_{refadj}) + R_{boot} + R_{ref2}]$
 $V_{out} = V_{min} + N * V_{step}$
 $V_{step} = (V_{max} - V_{min}) / N_{max}$

PWM VID and Output voltage control

- 1.Boot mode
- 2.Standby mode (don't support)
- 3.Normal mode



Remark:
1. Switching frequency setting:(Ton pin)
 $F_{sw} = (V_{in} - 0.5) / (2 * V_{in} * R_{ton} * 3.2p)$
 $= 352KHz$

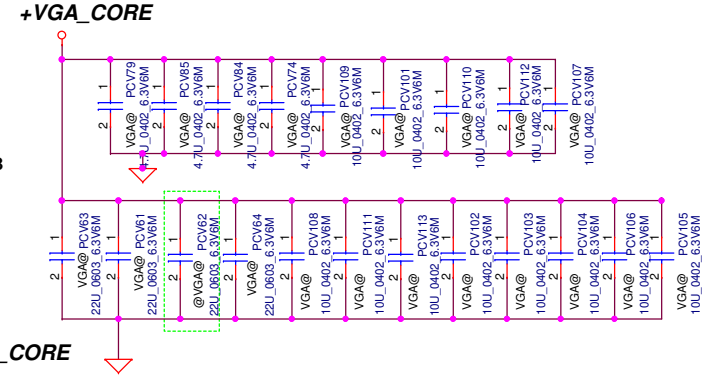
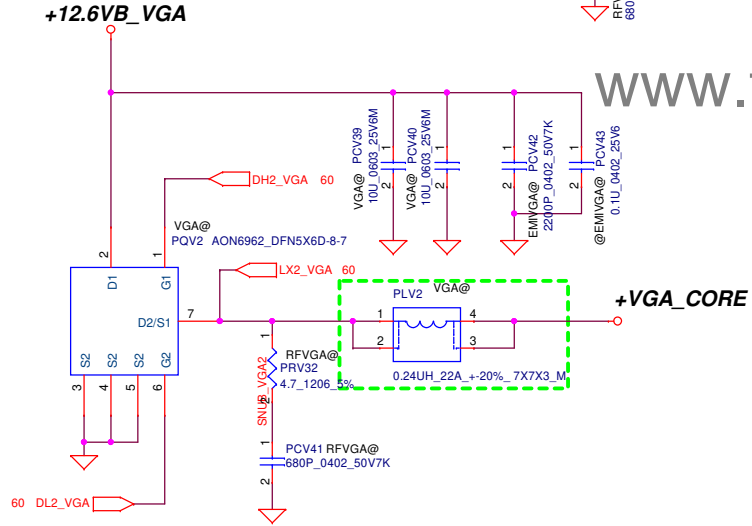
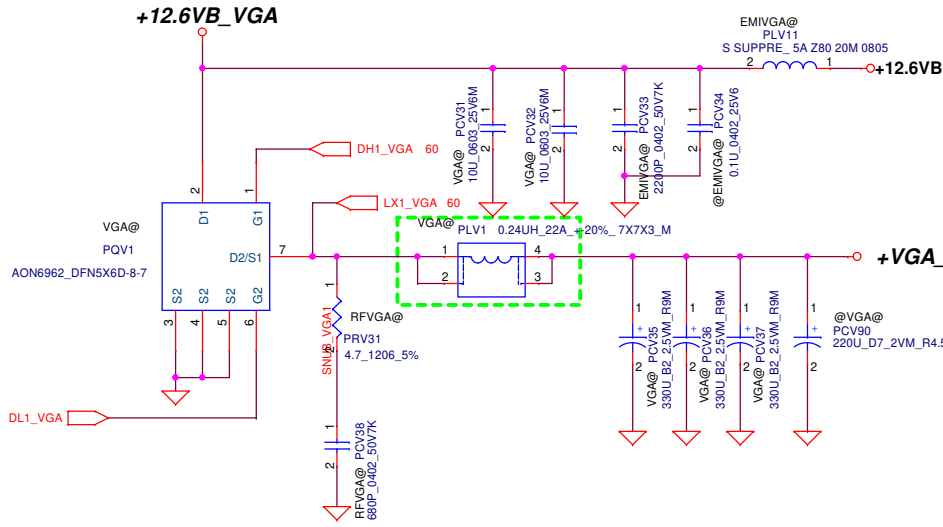
For debug only,
HW side need other resistor

Current Limit threshold setting
 $R_{ocset} = (I_{valley} * R_{ds(on)} * 12) / I_{coset}$

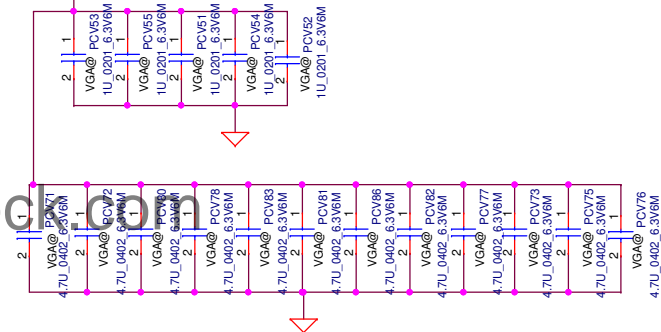
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Module model information:
RT8816A-2P_NVVDDS_V2A.mdd for IC portion
RT8816A-2P_NVVDDS_V2B.mdd for SW portion

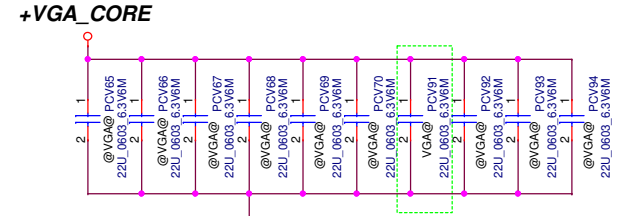
N17S-G2
+VGA_CORE
EDP-Continuous 28.6A
EDP-Peak 60.3A
OCP min A



+VGA_CORE
5M **GB4-128 package**



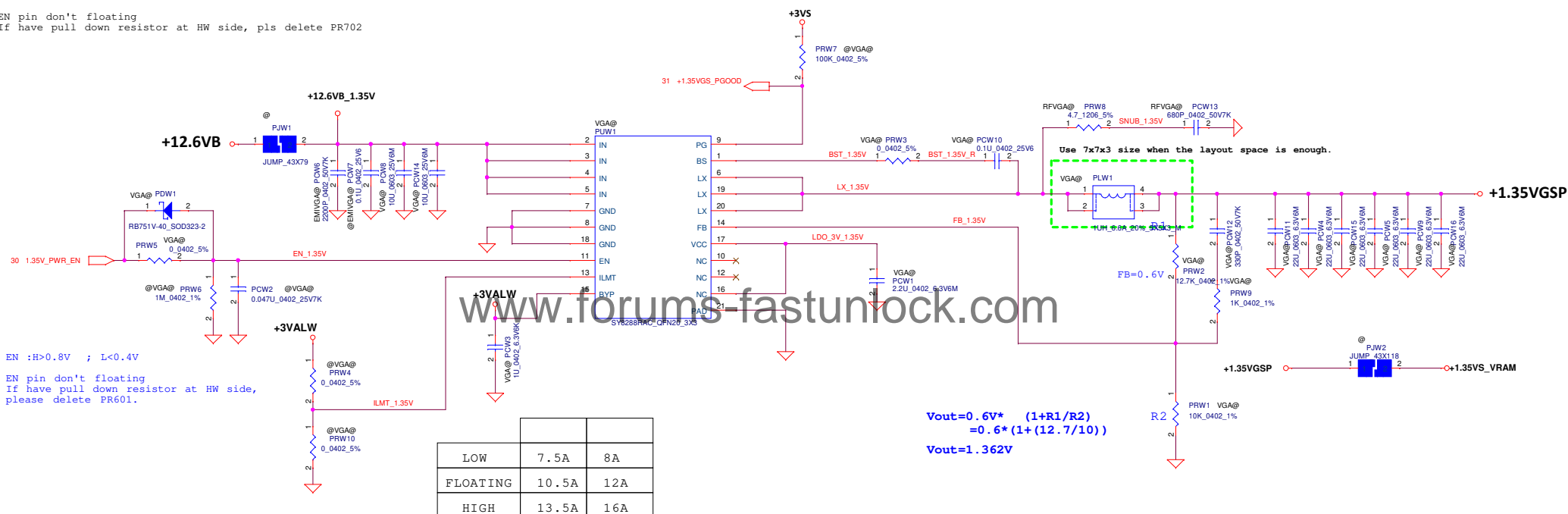
VGA_CORE output cap
330U_B2_2.5V 3pcs
22U_0603_6.3V 4pcs
4.7U_0402_6.3V 16pcs
10U_0603_6.3V 13pcs
1U_0402_16V 5pcs



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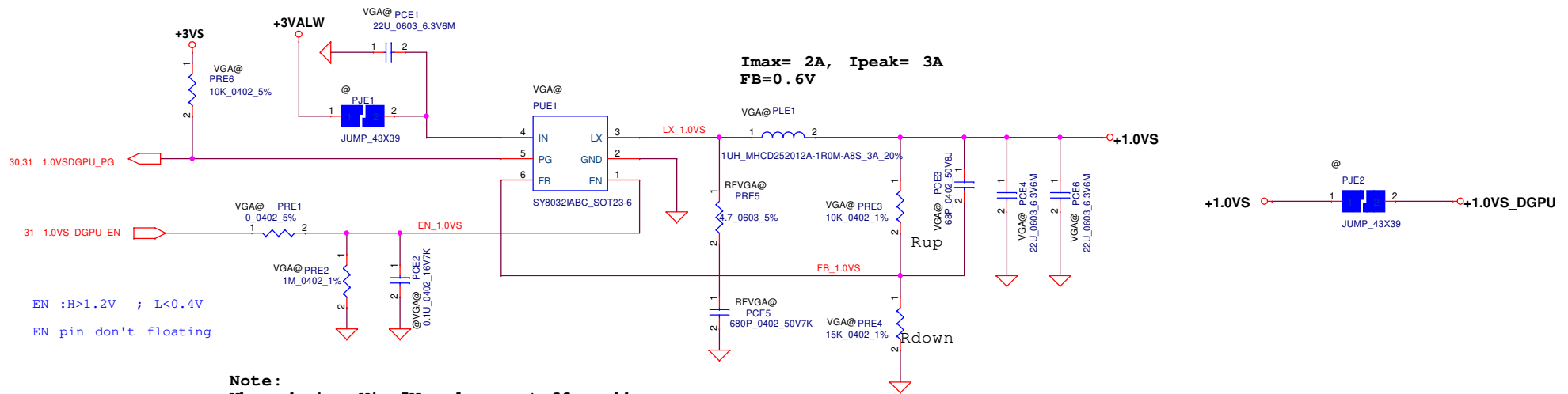

```
EN :H>0.8V ; L<0.4V
```

EN pin don't floating
If have pull down resistor at HW side,
please delete PR601.



LOW	7.5A	8A
FLOATING	10.5A	12A
HIGH	13.5A	16A

$$V_{out} = 0.6V * (1 + R_1/R_2)$$
$$= 0.6 * (1 + (12.7/10))$$
$$V_{out} = 1.362V$$

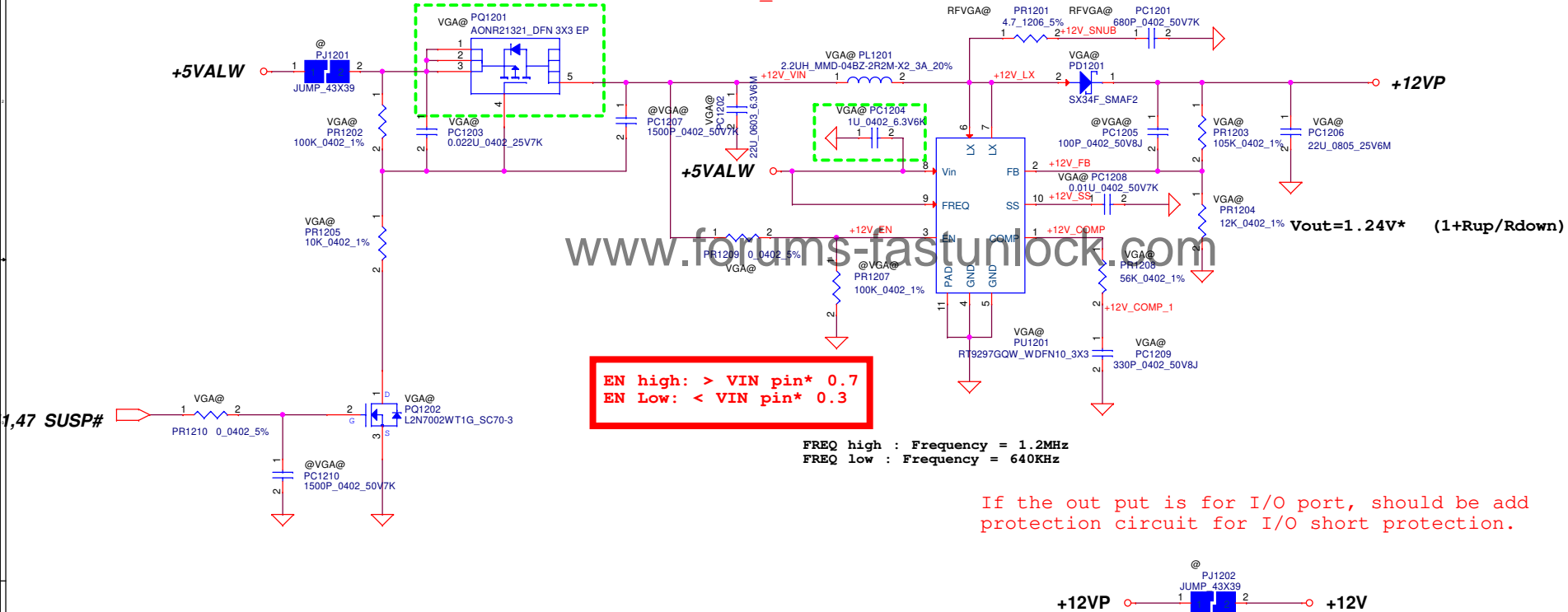


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RT9297_V1.mdd

Add a switch circuit to turn off the +12V_VIN if need.



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Item	Reason for change	PG#	Modify List	Date	Phase
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Version change list
(P.I.R. List)

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HW

Item	Reason for change	PG#	Modify List	Date	Phase
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